US

Fig. 1

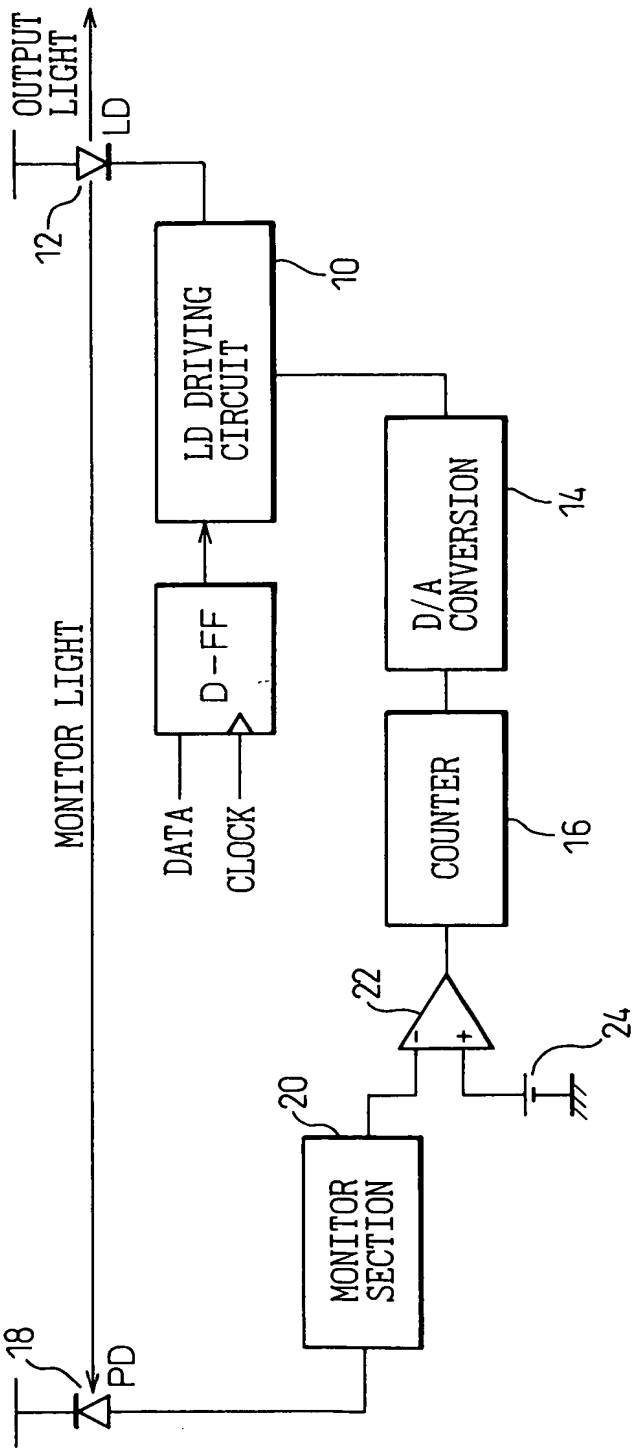

OUTPUT LIGHT
LD
12
LD DRIVING CIRCUIT
10
D-FF
DATA
CLOCK
MONITOR LIGHT
D/A CONVERSION
14
COUNTER
16
22
24
20
MONITOR SECTION
18
PD

Fig. 2

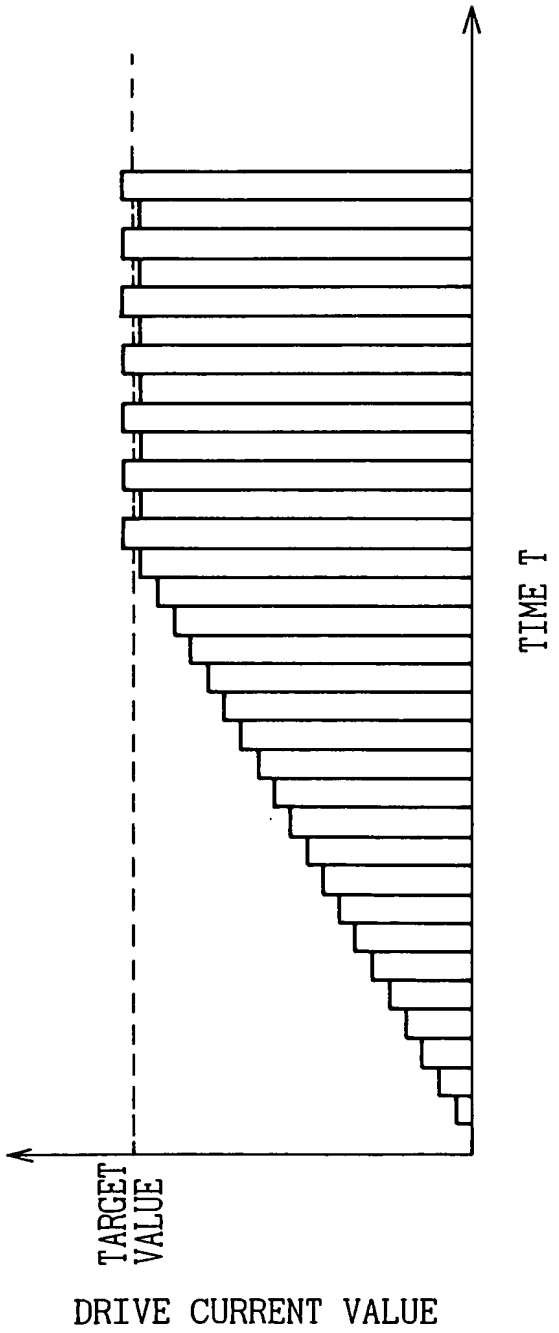


Fig.3

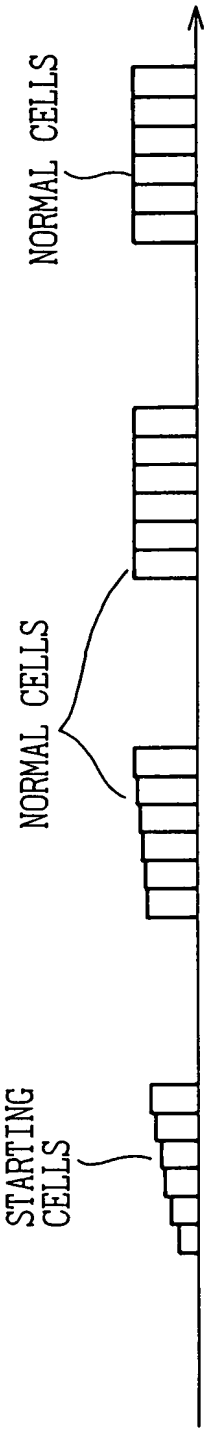


Fig. 4

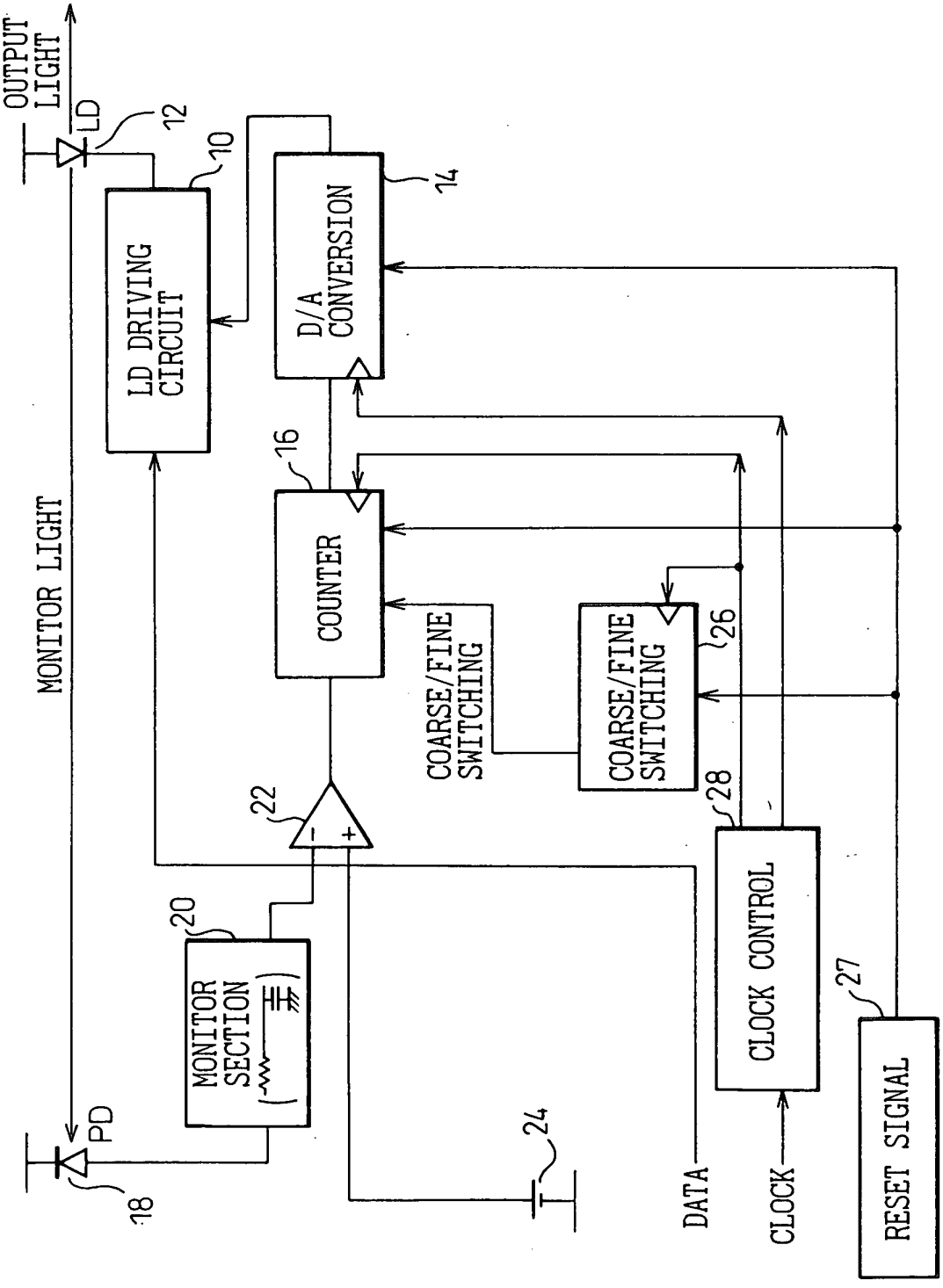

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
14
D/A CONVERSION
16
COUNTER
MONITOR LIGHT
COARSE/FINE SWITCHING
COARSE/FINE SWITCHING
26
22
28
20
MONITOR SECTION
CLOCK CONTROL
27
PD
18
24
DATA
CLOCK
RESET SIGNAL

Fig.5

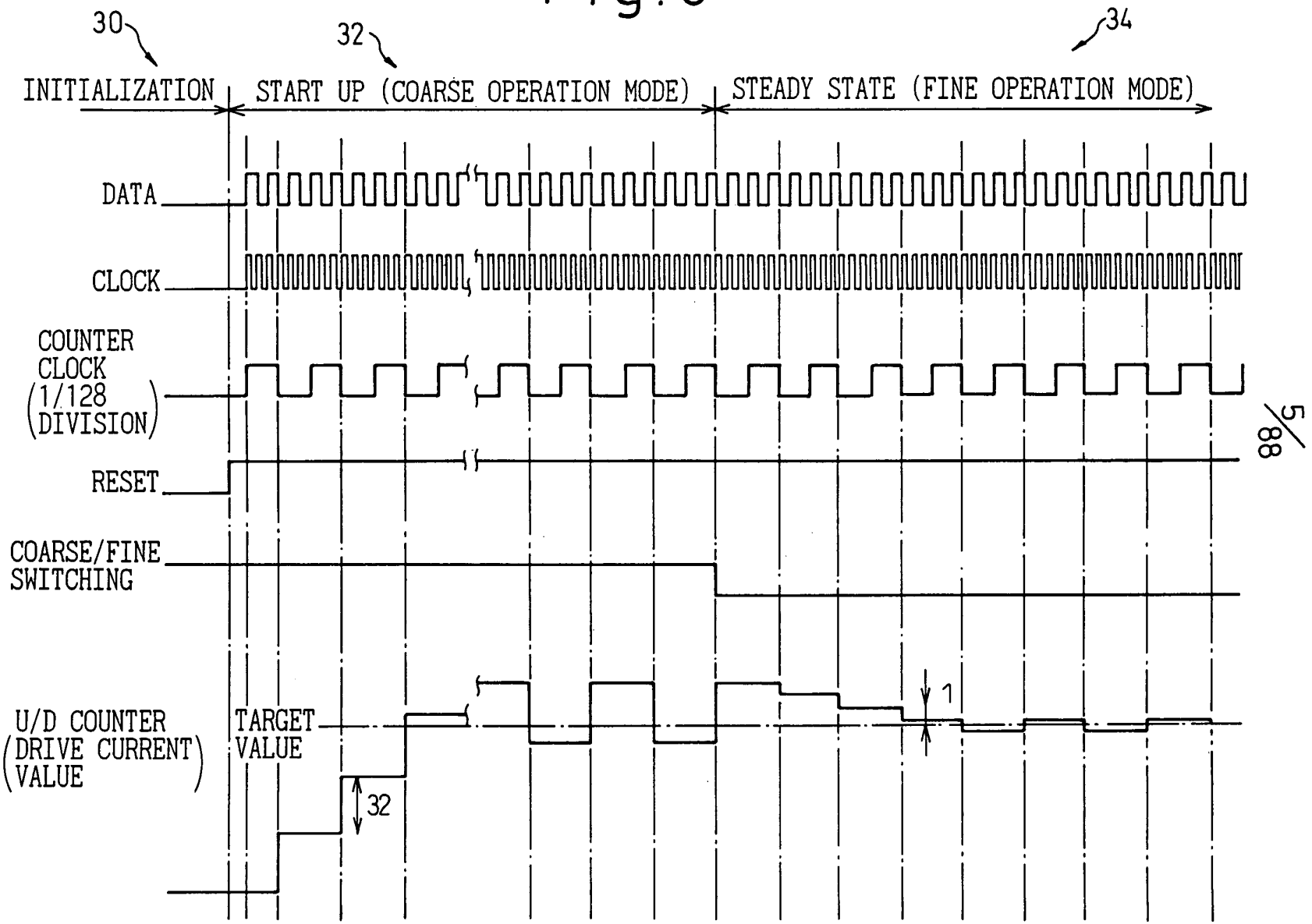

30
32
34
INITIALIZATION
START UP (COARSE OPERATION MODE)
STEADY STATE (FINE OPERATION MODE)
DATA
CLOCK
COUNTER CLOCK (1/128 DIVISION)
RESET
COARSE/FINE SWITCHING
U/D COUNTER (DRIVE CURRENT VALUE)
TARGET VALUE
32
1

Fig. 6

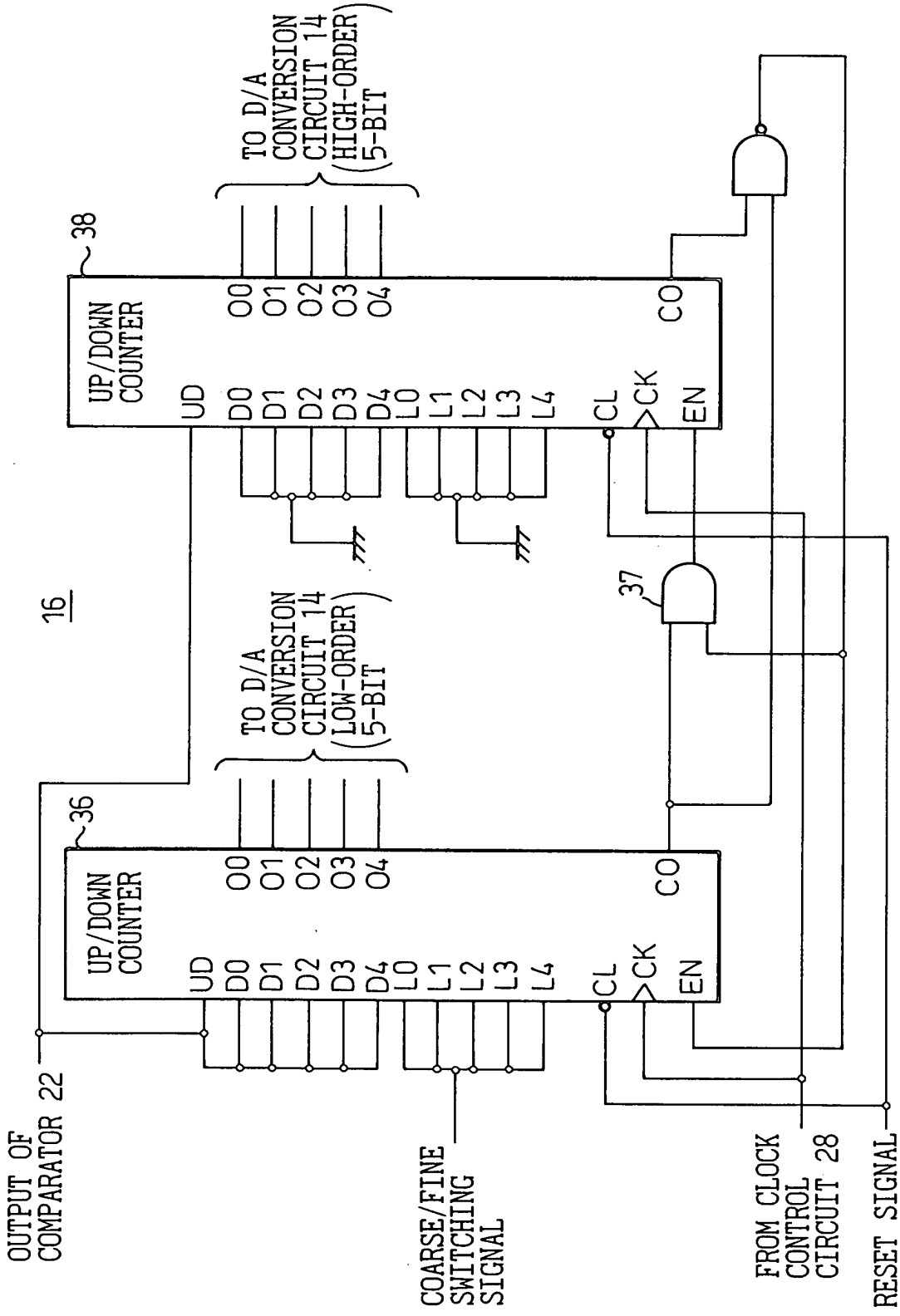

16
38
UP/DOWN COUNTER
UD
D0
D1
D2
D3
D4
L0
L1
L2
L3
L4
CL
CK
EN
O0
O1
O2
O3
O4
CO
TO D/A CONVERSION CIRCUIT 14 (HIGH-ORDER 5-BIT)
36
TO D/A CONVERSION CIRCUIT 14 (LOW-ORDER 5-BIT)
37
OUTPUT OF COMPARATOR 22
COARSE/FINE SWITCHING SIGNAL
FROM CLOCK CONTROL CIRCUIT 28
RESET SIGNAL

Fig.7

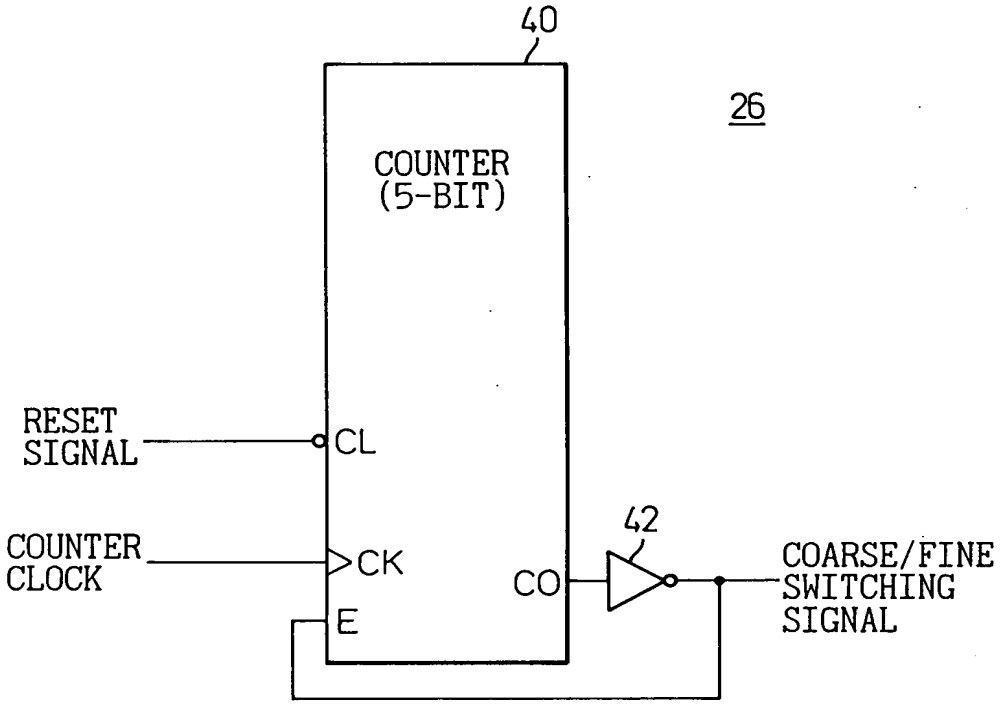

40
26
COUNTER
(5-BIT)
RESET
SIGNAL
CL
COUNTER
CLOCK
CK
E
CO
42
COARSE/FINE
SWITCHING
SIGNAL

Fig.8

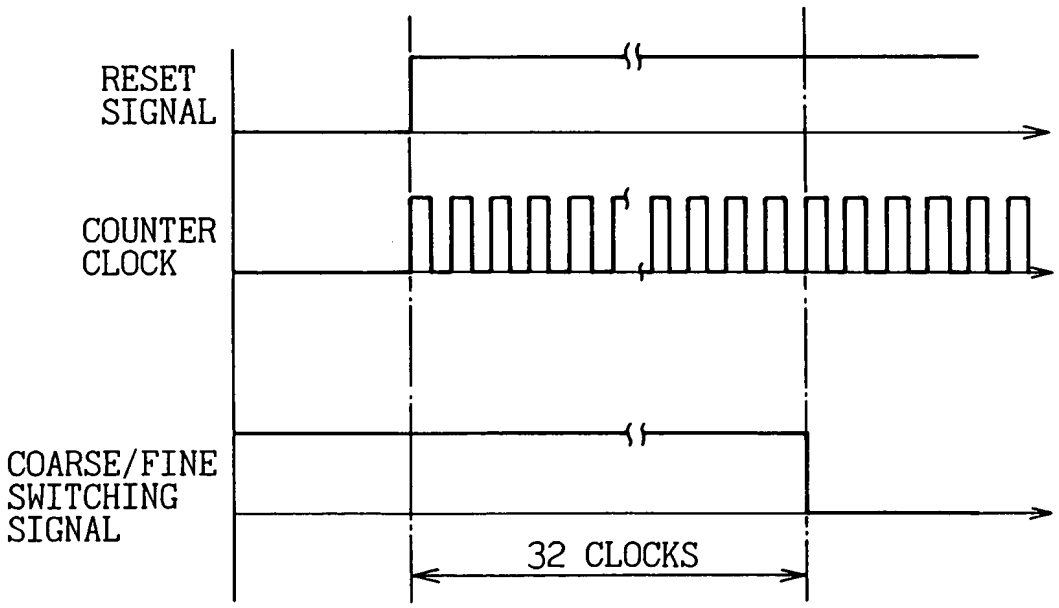

RESET
SIGNAL
COUNTER
CLOCK
COARSE/FINE
SWITCHING
SIGNAL
32 CLOCKS

Fig.9

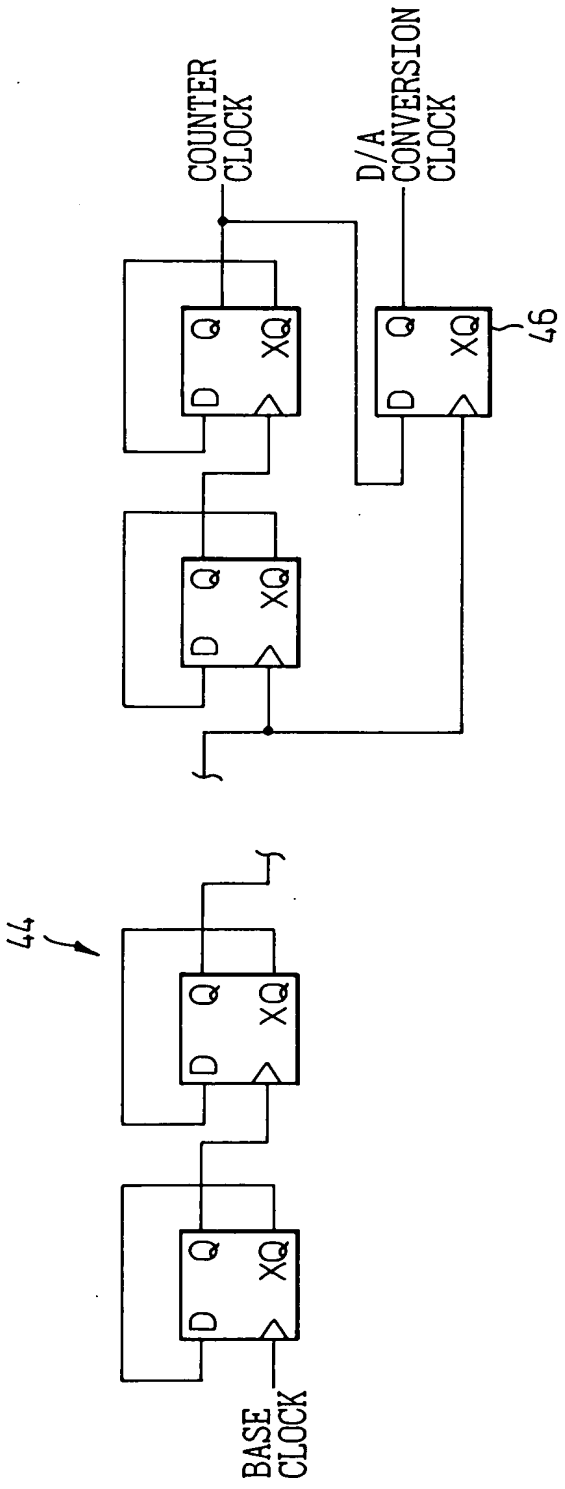


Fig.10

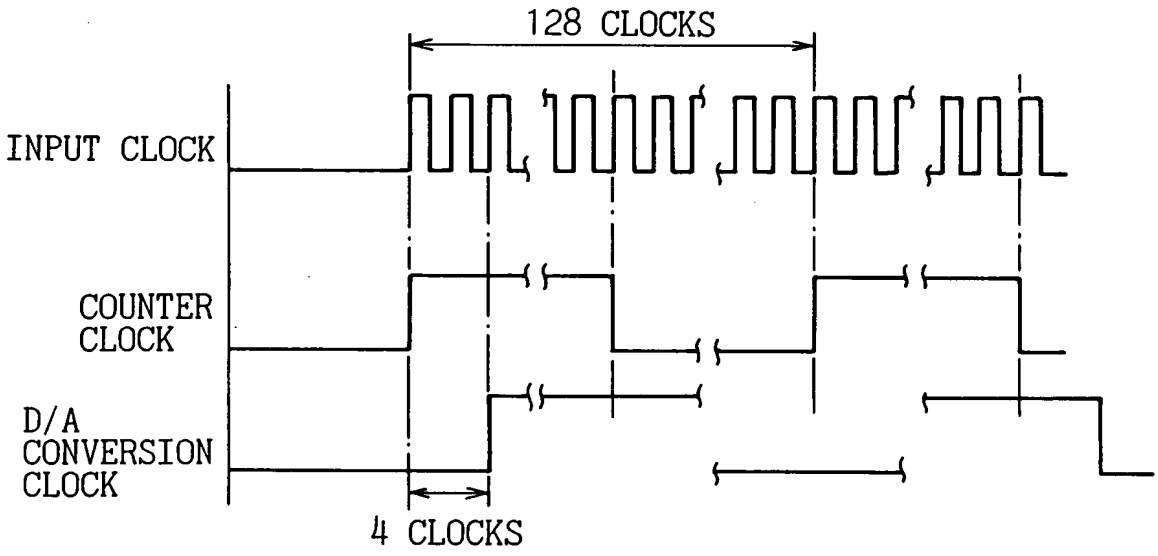

128 CLOCKS
INPUT CLOCK
COUNTER CLOCK
D/A CONVERSION CLOCK
4 CLOCKS

Fig.11

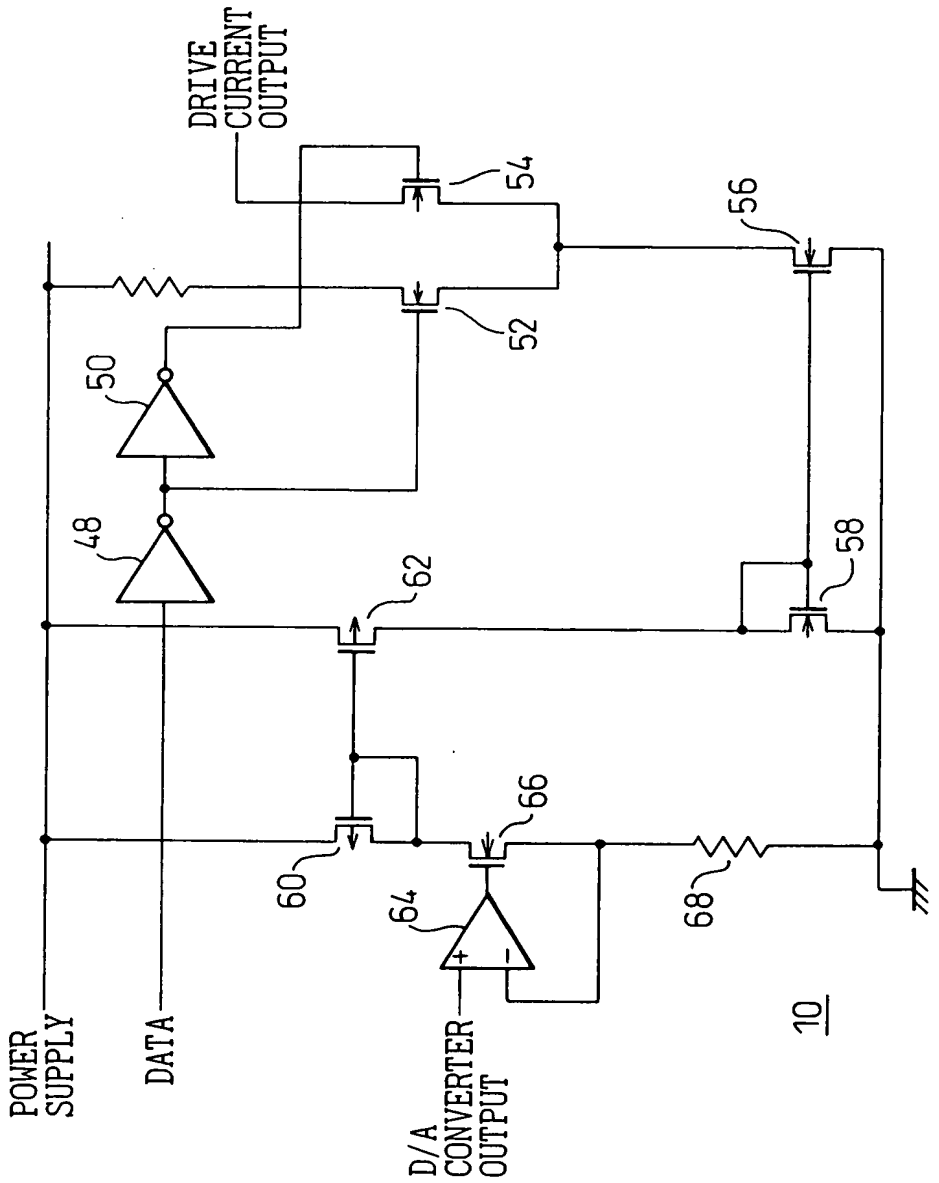

DRIVE CURRENT OUTPUT
54
56
52
50
48
62
58
66
60
64
68
POWER SUPPLY
DATA
D/A CONVERTER OUTPUT
10

Fig.12

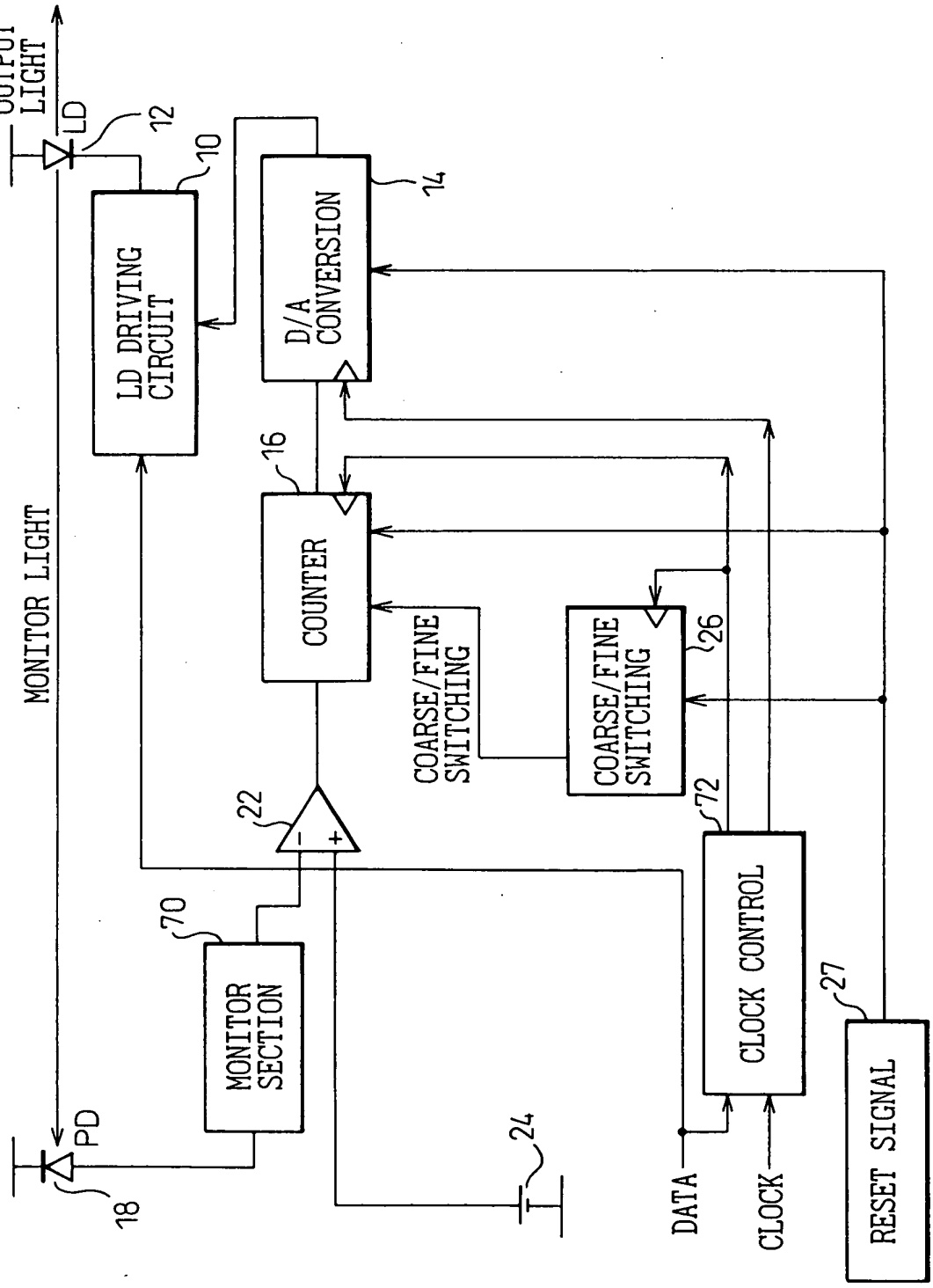

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
D/A CONVERSION
14
16
COUNTER
MONITOR LIGHT
COARSE/FINE SWITCHING
COARSE/FINE SWITCHING
26
22
72
70
MONITOR SECTION
CLOCK CONTROL
27
PD
18
24
DATA
CLOCK
RESET SIGNAL

Fig.13

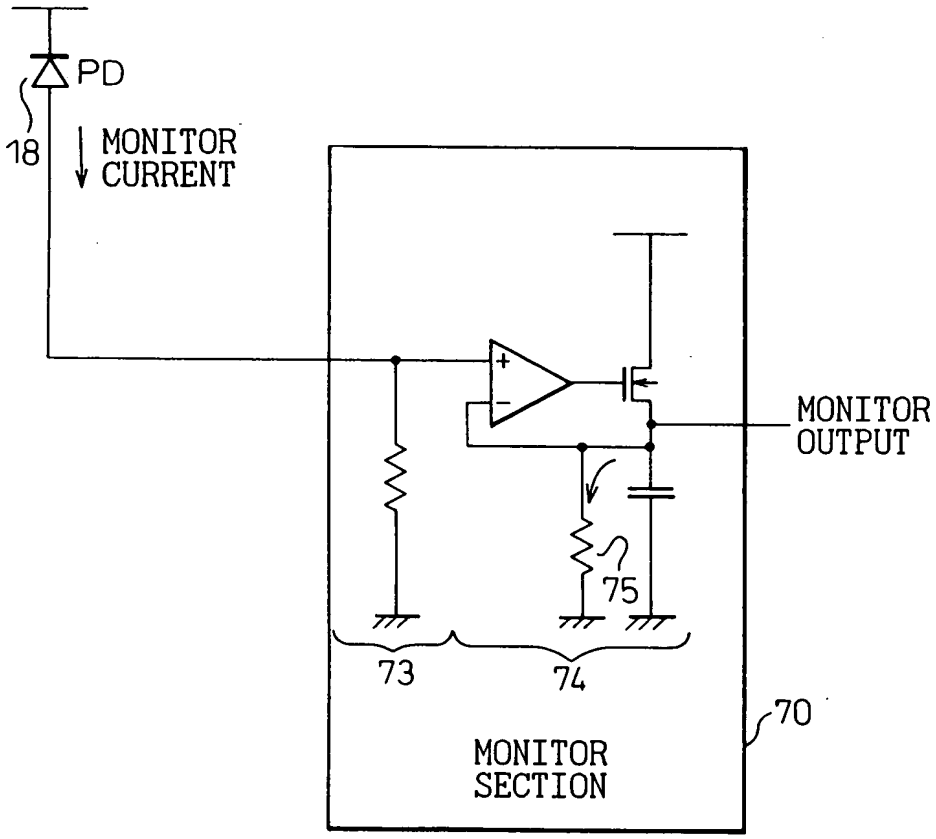

PD
18
MONITOR
CURRENT
MONITOR
OUTPUT
75
73
74
70
MONITOR
SECTION

Fig.14

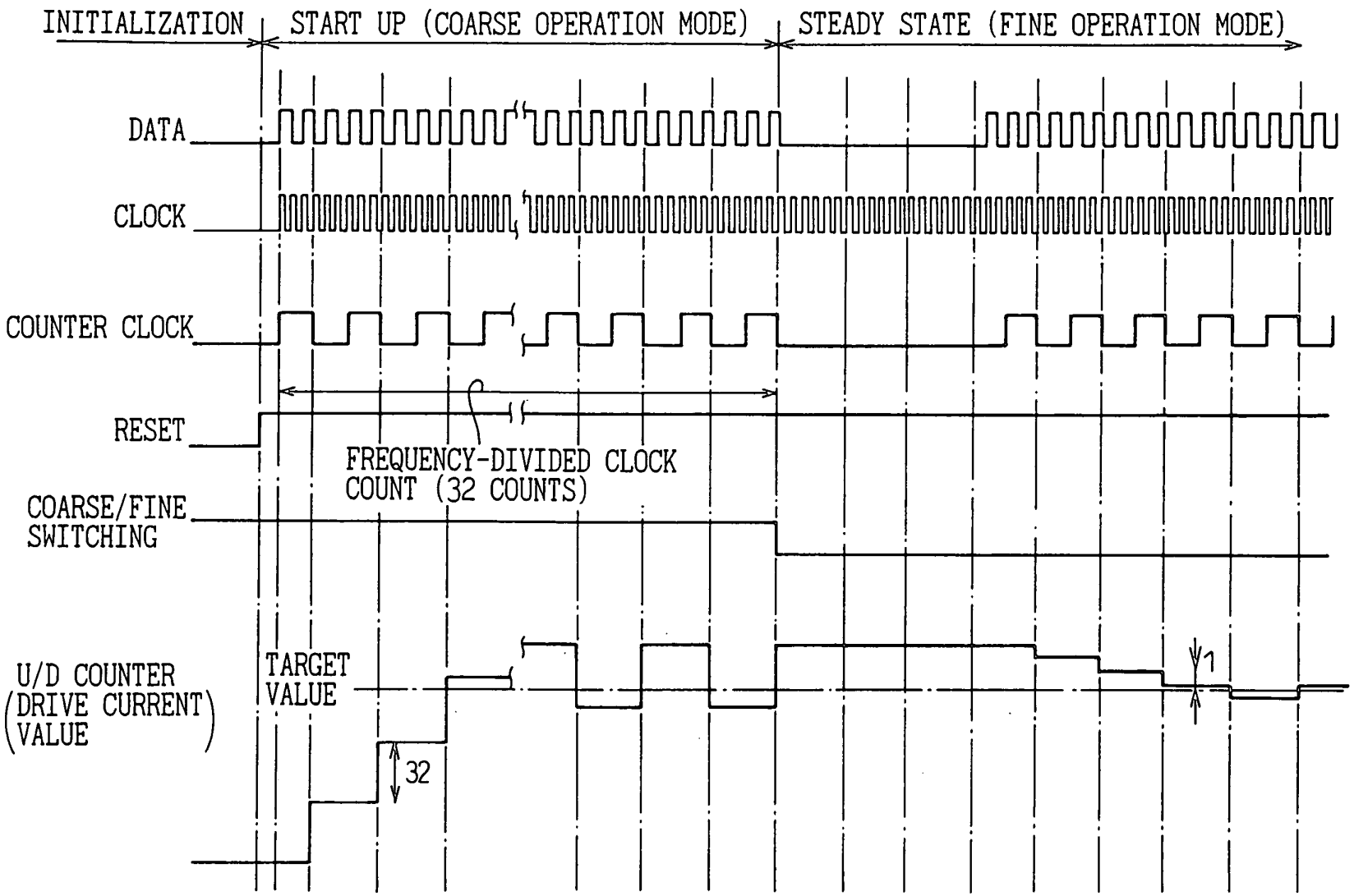

INITIALIZATION
START UP (COARSE OPERATION MODE)
STEADY STATE (FINE OPERATION MODE)
DATA
CLOCK
COUNTER CLOCK
RESET
FREQUENCY-DIVIDED CLOCK COUNT (32 COUNTS)
COARSE/FINE SWITCHING
U/D COUNTER (DRIVE CURRENT VALUE)
TARGET VALUE
32
1

Fig.15

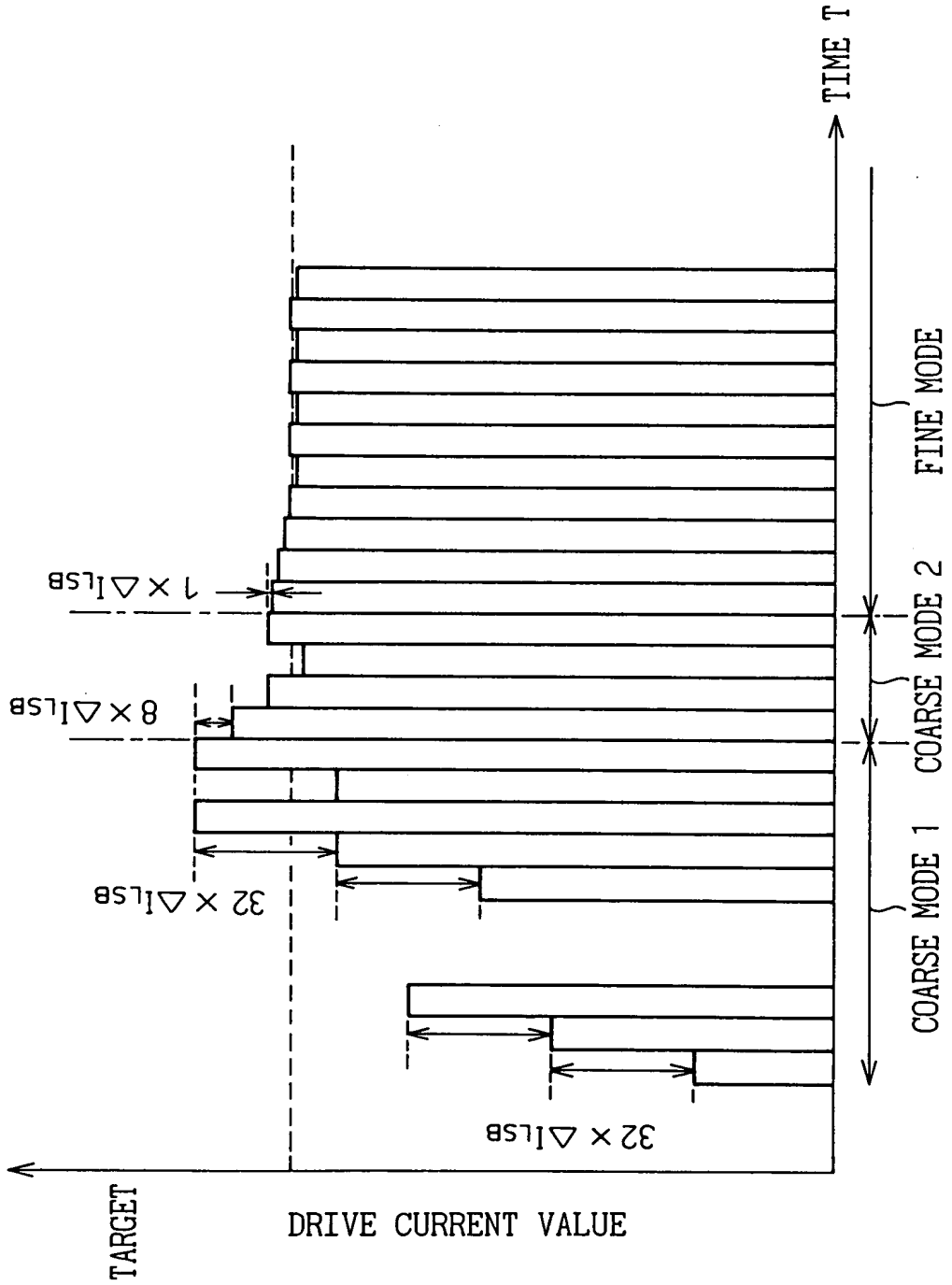

TIME T
FINE MODE
COARSE MODE 2
COARSE MODE 1
1 × ΔILSB
8 × ΔILSB
32 × ΔILSB
32 × ΔILSB
TARGET
DRIVE CURRENT VALUE

Fig.16

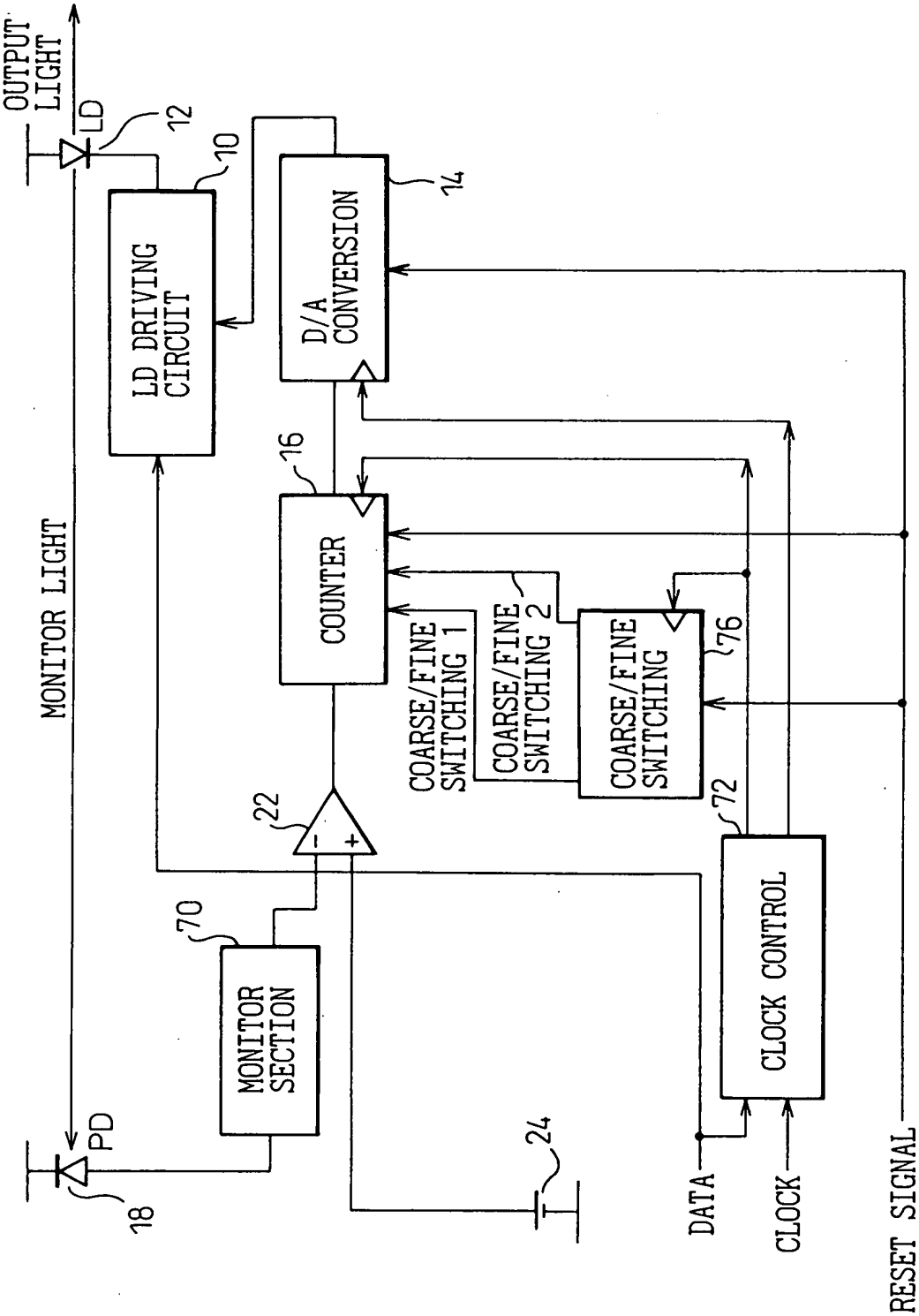

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
D/A CONVERSION
14
16
COUNTER
MONITOR LIGHT
COARSE/FINE SWITCHING 1
COARSE/FINE SWITCHING 2
COARSE/FINE SWITCHING
76
72
22
70
MONITOR SECTION
CLOCK CONTROL
PD
18
24
DATA
CLOCK
RESET SIGNAL

Fig.17

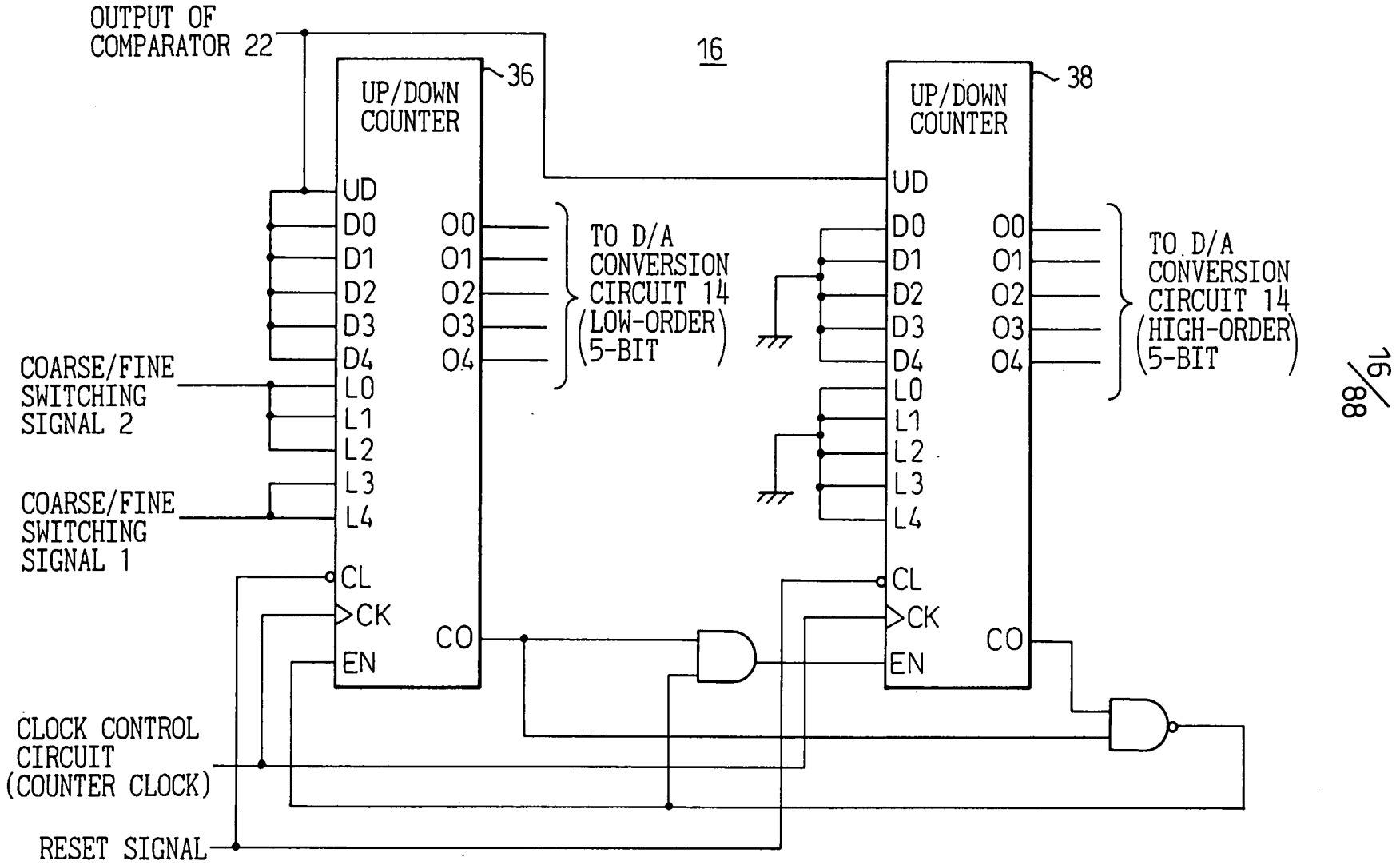

OUTPUT OF COMPARATOR 22
16
UP/DOWN COUNTER
36
UP/DOWN COUNTER
38
UD
D0
D1
D2
D3
D4
L0
L1
L2
L3
L4
CL
CK
EN
O0
O1
O2
O3
O4
CO
TO D/A CONVERSION CIRCUIT 14 (LOW-ORDER 5-BIT)
TO D/A CONVERSION CIRCUIT 14 (HIGH-ORDER 5-BIT)
COARSE/FINE SWITCHING SIGNAL 2
COARSE/FINE SWITCHING SIGNAL 1
CLOCK CONTROL CIRCUIT (COUNTER CLOCK)
RESET SIGNAL

Fig.18

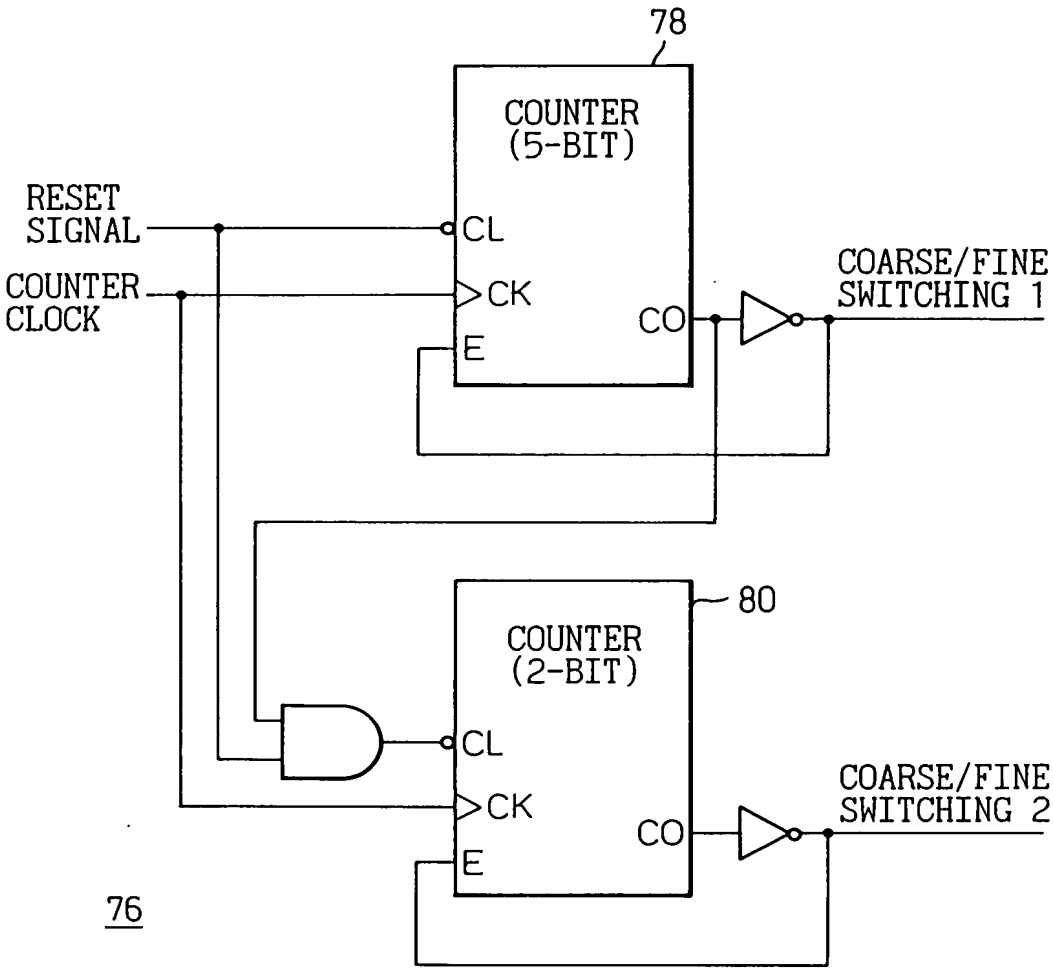

78
COUNTER
(5-BIT)
RESET
SIGNAL
CL
COUNTER
CLOCK
CK
CO
E
COARSE/FINE
SWITCHING 1
80
COUNTER
(2-BIT)
CL
CK
CO
E
COARSE/FINE
SWITCHING 2
76

Fig.19

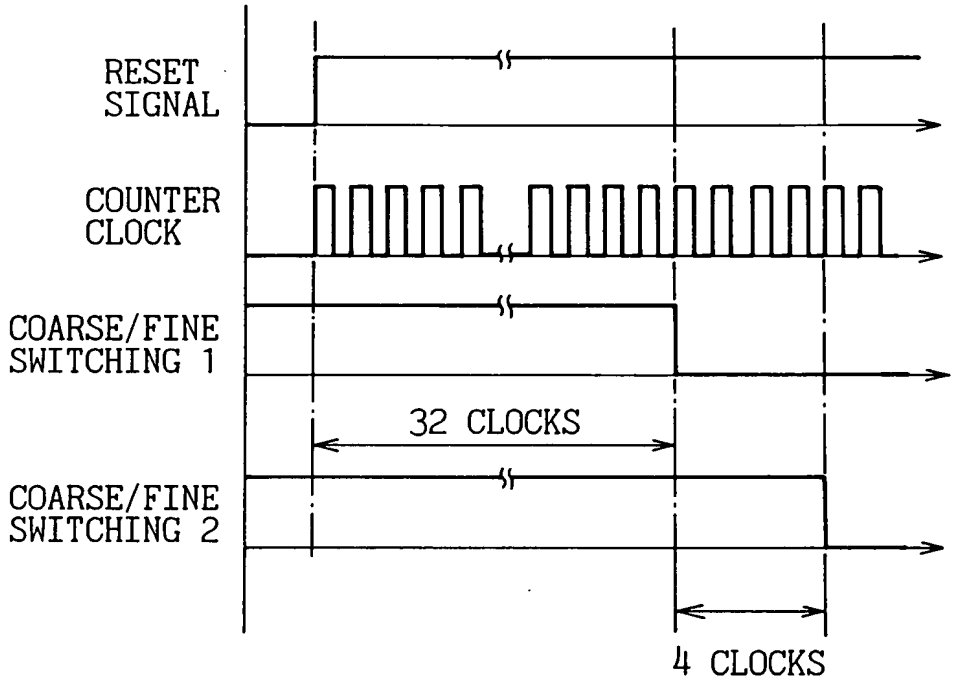

RESET SIGNAL
COUNTER CLOCK
COARSE/FINE SWITCHING 1
32 CLOCKS
COARSE/FINE SWITCHING 2
4 CLOCKS

Fig.20

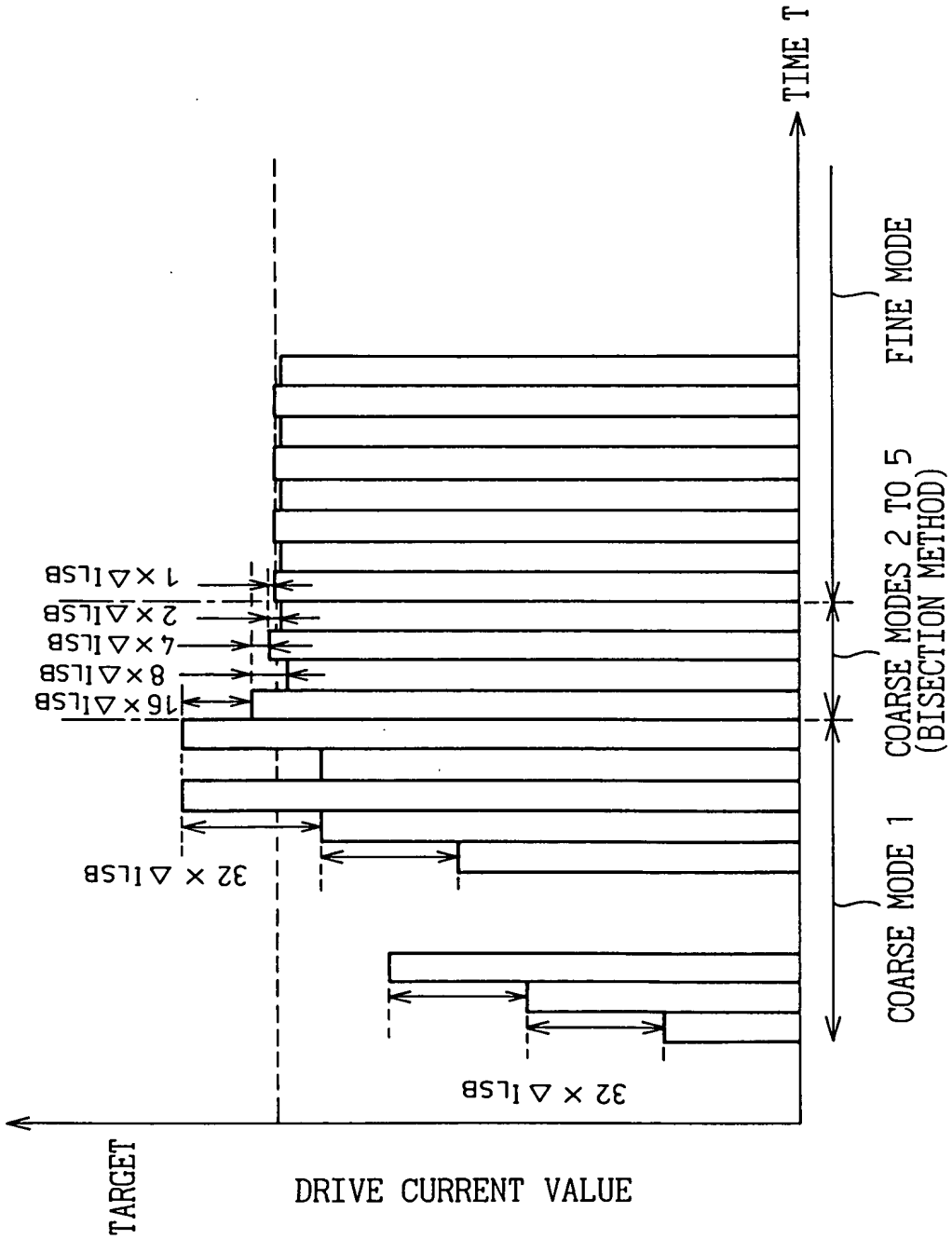

TIME T
FINE MODE
COARSE MODES 2 TO 5
(BISECTION METHOD)
COARSE MODE 1
1 × ΔILSB
2 × ΔILSB
4 × ΔILSB
8 × ΔILSB
16 × ΔILSB
32 × ΔILSB
32 × ΔILSB
TARGET
DRIVE CURRENT VALUE

Fig.21

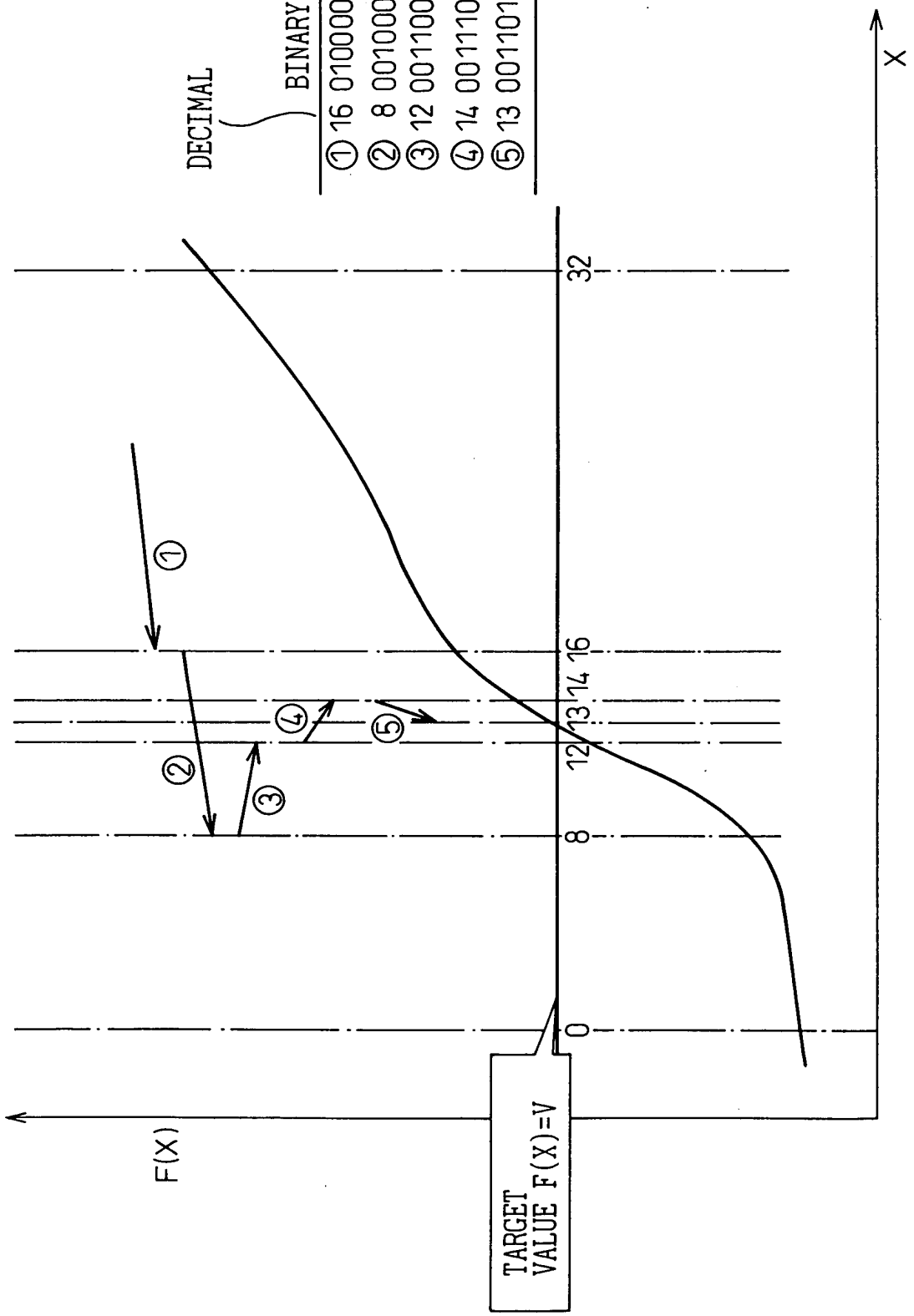

DECIMAL
BINARY
① 16 010000
② 8 001000
③ 12 001100
④ 14 001110
⑤ 13 001101
X
F(X)
TARGET VALUE F(X)=V
0
8
12
13
14
16
32
①
②
③
④
⑤

Fig.22

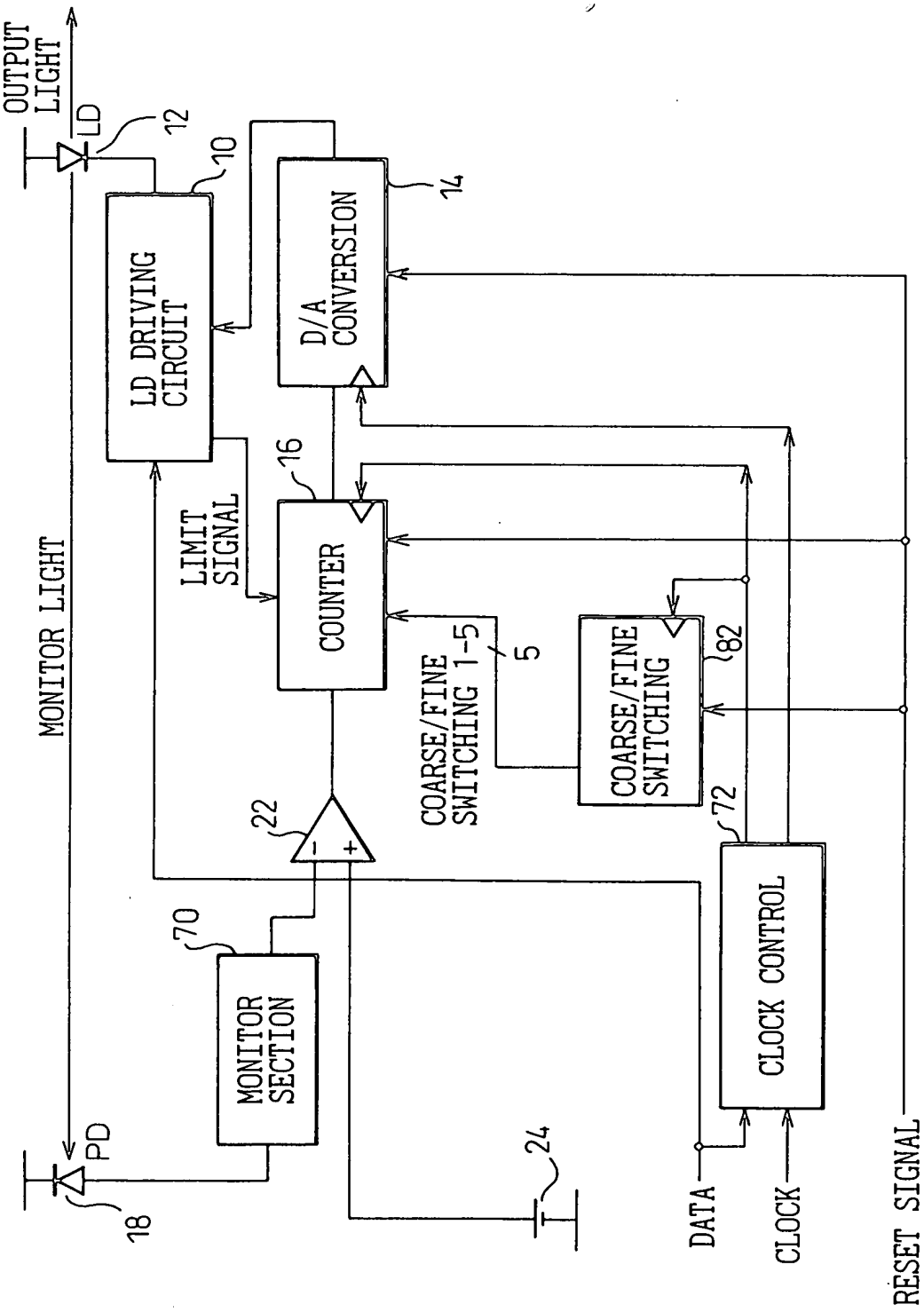

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
D/A CONVERSION
14
16
LIMIT SIGNAL
COUNTER
MONITOR LIGHT
COARSE/FINE SWITCHING 1-5
5
COARSE/FINE SWITCHING
82
72
22
-
+
CLOCK CONTROL
70
MONITOR SECTION
PD
18
24
DATA
CLOCK
RESET SIGNAL

Fig.23

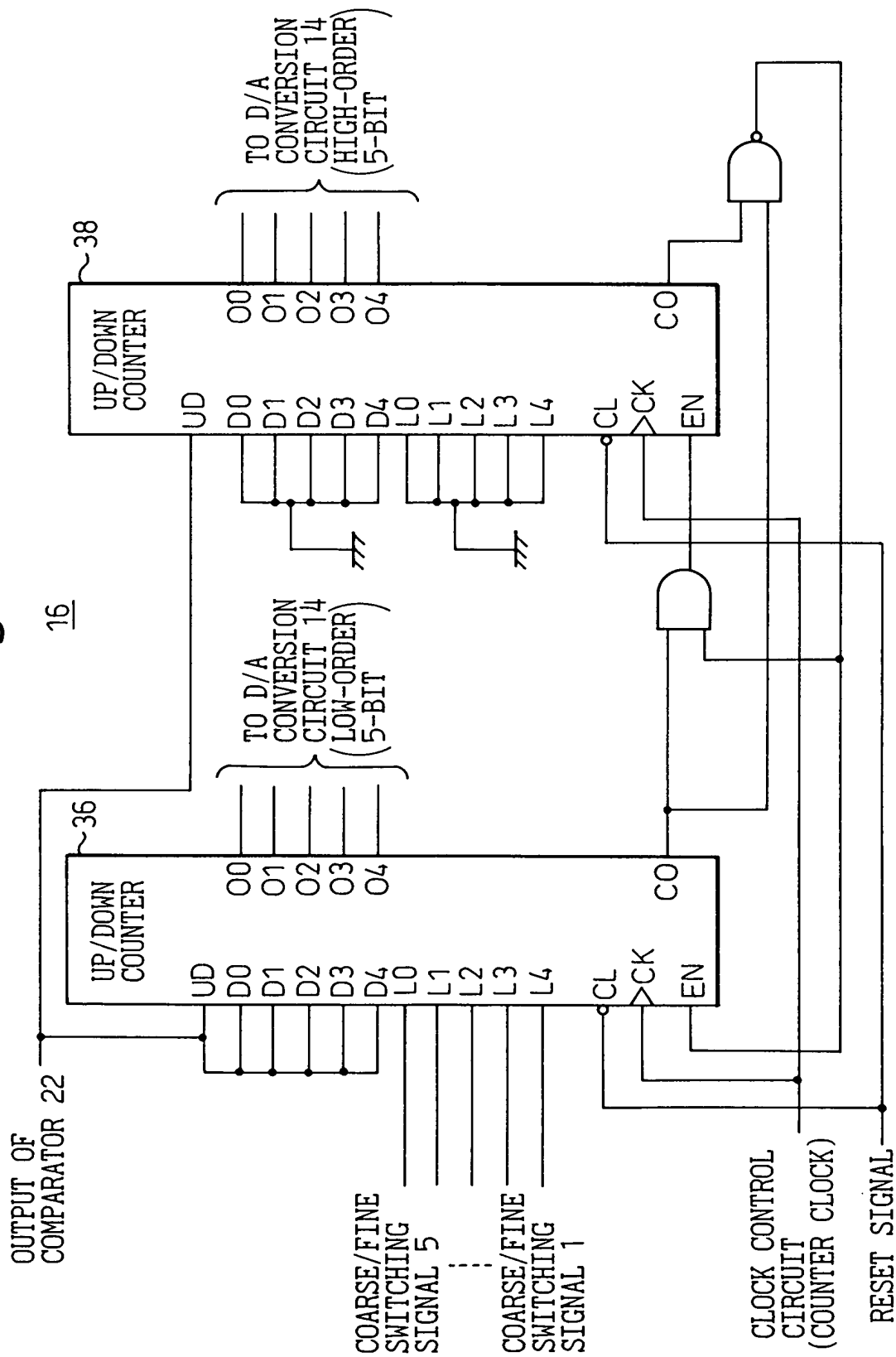

16
38
UP/DOWN COUNTER
UD
D0
D1
D2
D3
D4
L0
L1
L2
L3
L4
CL
CK
EN
O0
O1
O2
O3
O4
CO
TO D/A CONVERSION CIRCUIT 14 (HIGH-ORDER 5-BIT)
36
UP/DOWN COUNTER
TO D/A CONVERSION CIRCUIT 14 (LOW-ORDER 5-BIT)
OUTPUT OF COMPARATOR 22
COARSE/FINE SWITCHING SIGNAL 5
COARSE/FINE SWITCHING SIGNAL 1
CLOCK CONTROL CIRCUIT (COUNTER CLOCK)
RESET SIGNAL

Fig.24

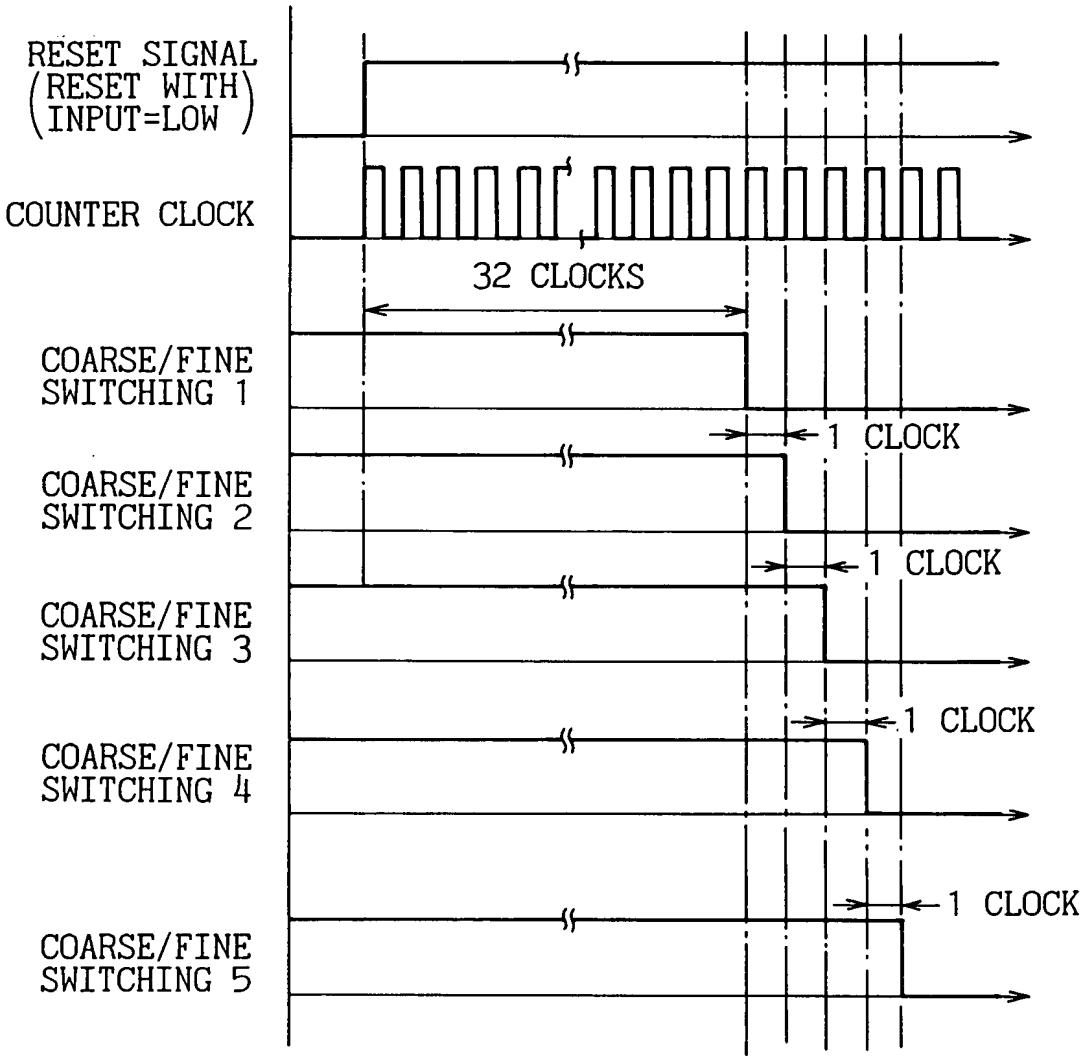

RESET SIGNAL
(RESET WITH
INPUT=LOW)
COUNTER CLOCK
32 CLOCKS
COARSE/FINE
SWITCHING 1
1 CLOCK
COARSE/FINE
SWITCHING 2
1 CLOCK
COARSE/FINE
SWITCHING 3
1 CLOCK
COARSE/FINE
SWITCHING 4
1 CLOCK
COARSE/FINE
SWITCHING 5

Fig. 25

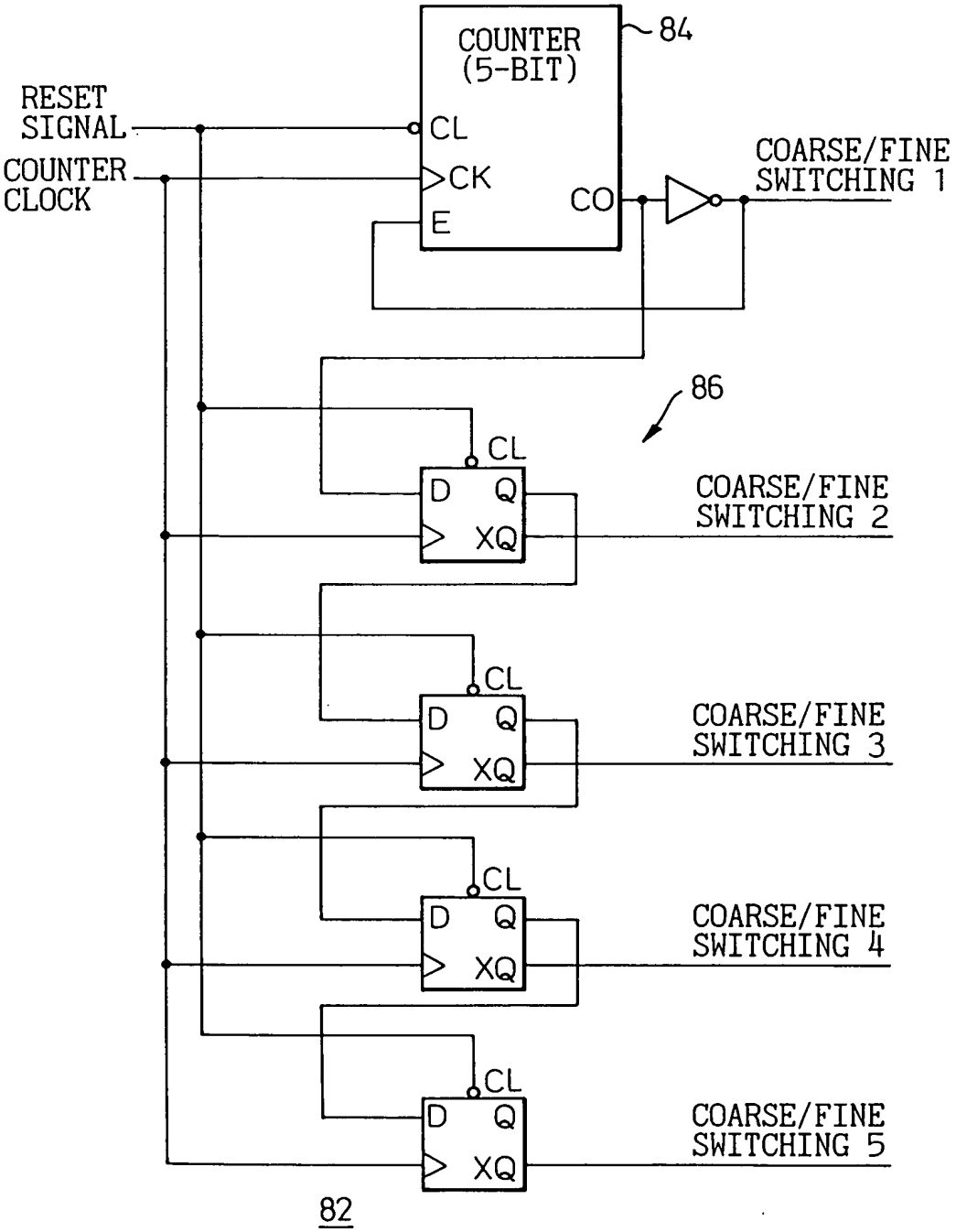

COUNTER
(5-BIT)
84
RESET
SIGNAL
COUNTER
CLOCK
CL
CK
E
CO
COARSE/FINE
SWITCHING 1
86
CL
D
Q
XQ
COARSE/FINE
SWITCHING 2
CL
D
Q
XQ
COARSE/FINE
SWITCHING 3
CL
D
Q
XQ
COARSE/FINE
SWITCHING 4
CL
D
Q
XQ
COARSE/FINE
SWITCHING 5
82

Fig.26

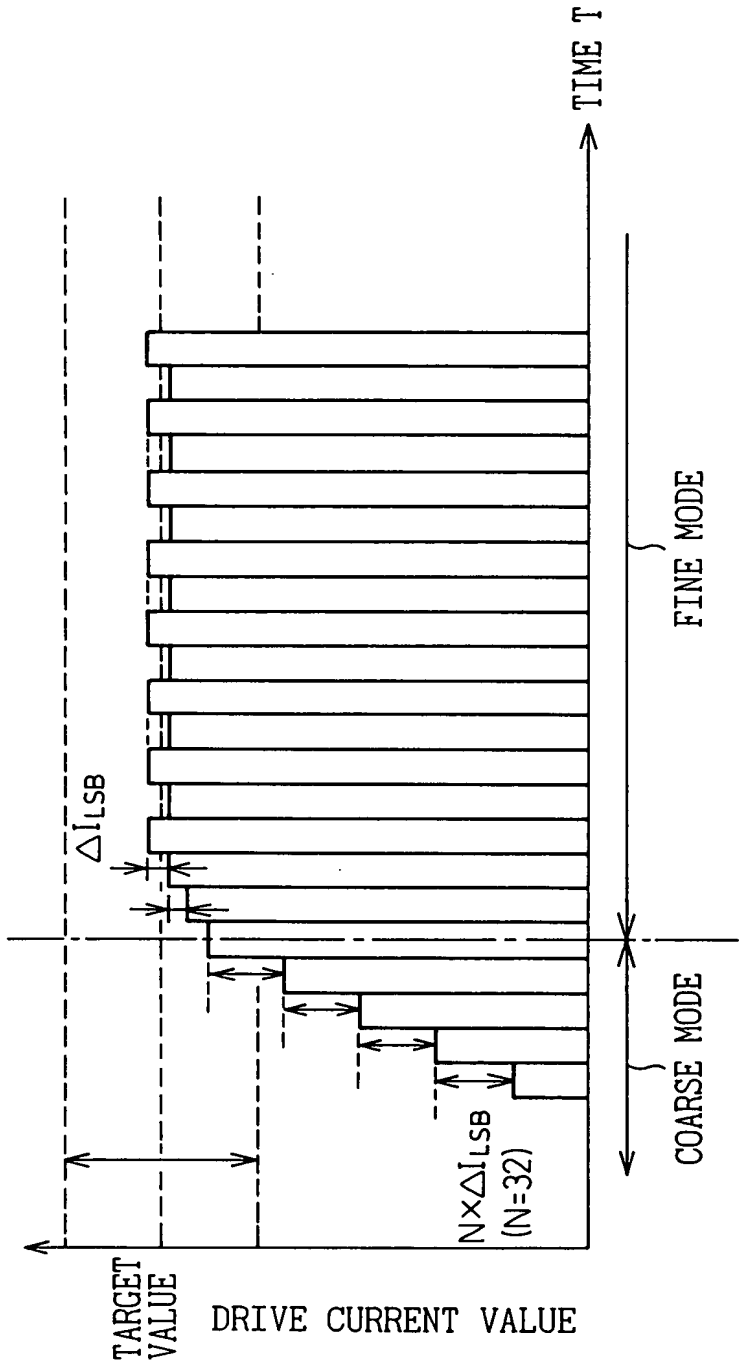

TIME T
FINE MODE
COARSE MODE
ΔILSB
N×ΔILSB
(N=32)
TARGET VALUE
DRIVE CURRENT VALUE

Fig.27

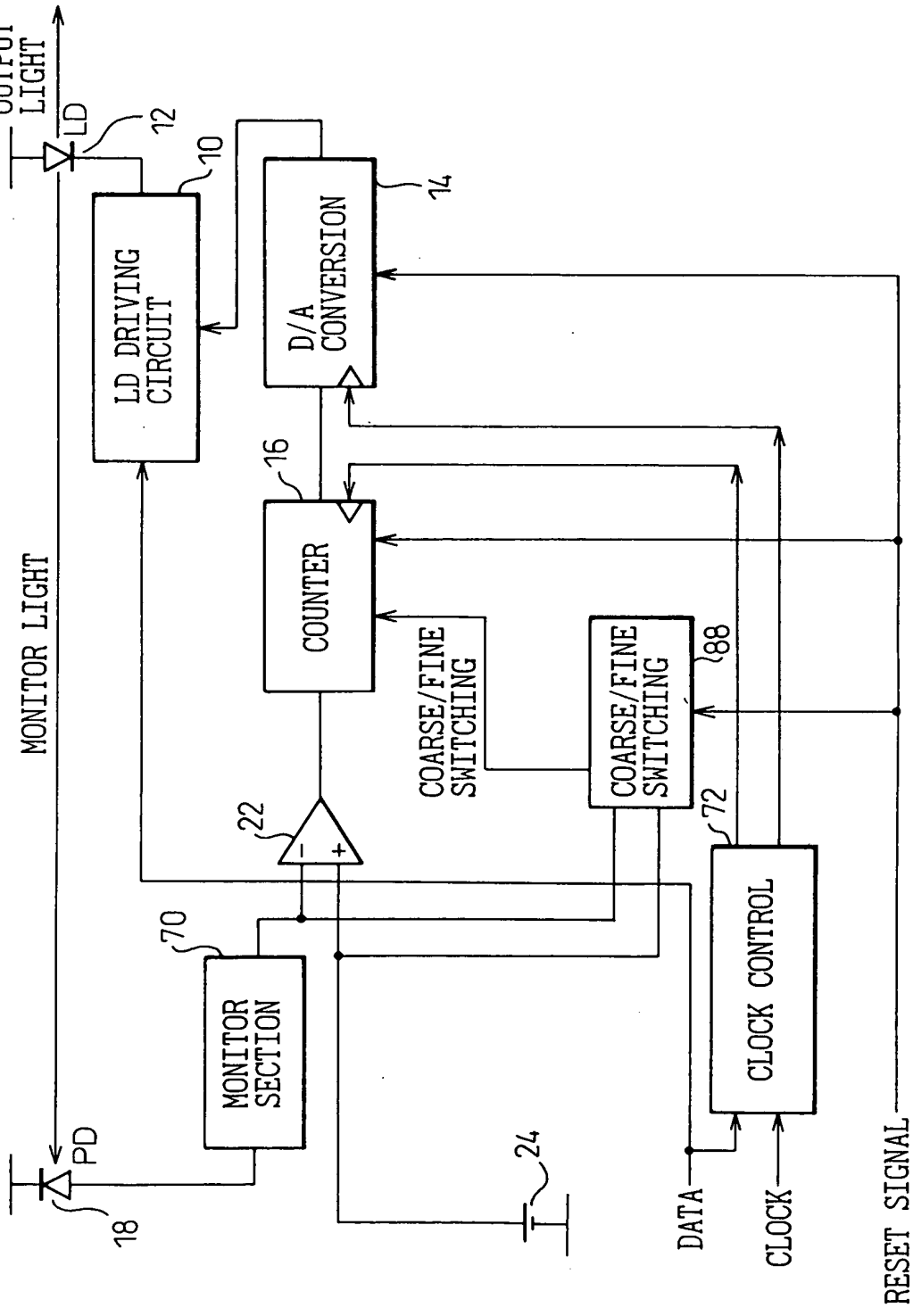

OUTPUT LIGHT
LD
12
10
14
LD DRIVING CIRCUIT
D/A CONVERSION
16
COUNTER
MONITOR LIGHT
COARSE/FINE SWITCHING
COARSE/FINE SWITCHING
88
22
72
70
MONITOR SECTION
CLOCK CONTROL
PD
18
24
DATA
CLOCK
RESET SIGNAL

Fig.28

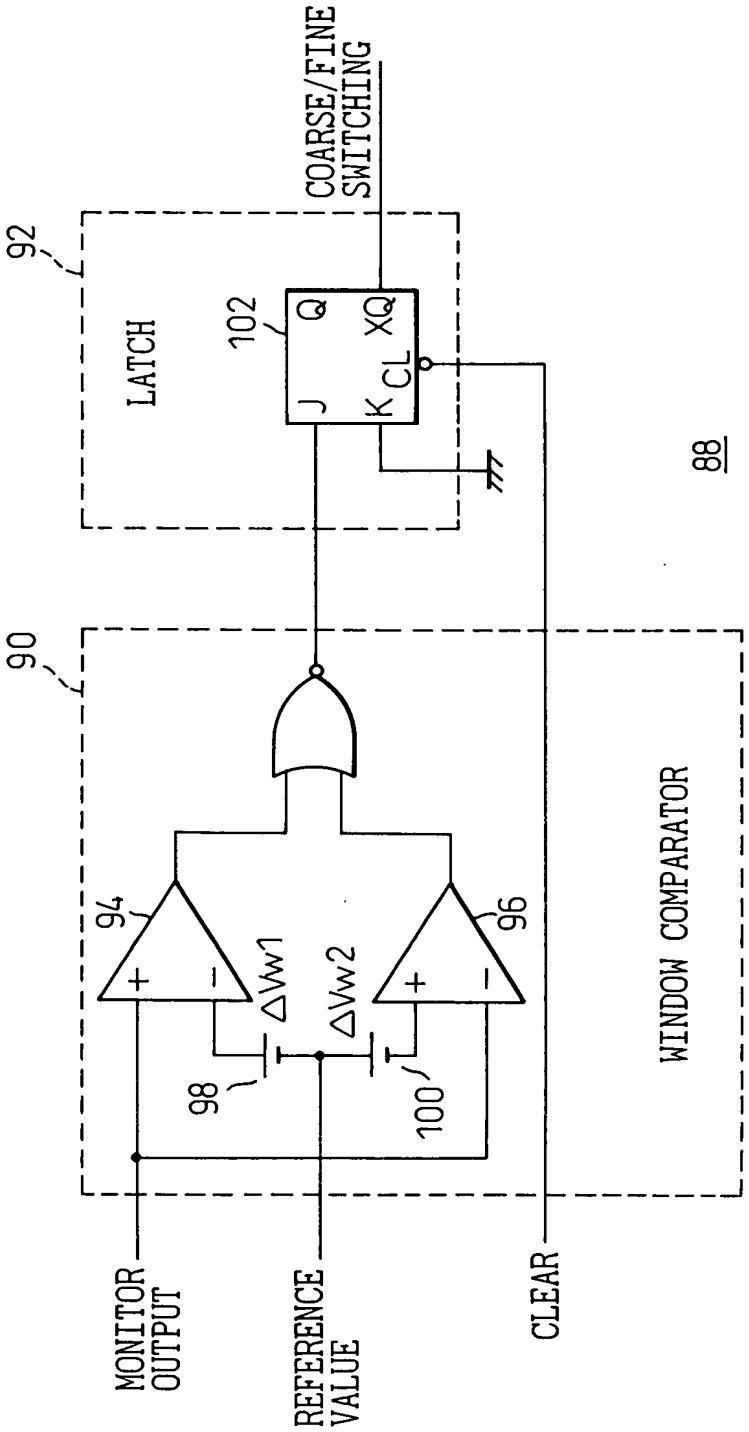

COARSE/FINE SWITCHING
92
LATCH
102
Q
XQ
J
K
CL
88
90
94
96
ΔVw1
ΔVw2
98
100
WINDOW COMPARATOR
MONITOR OUTPUT
REFERENCE VALUE
CLEAR

Fig. 29

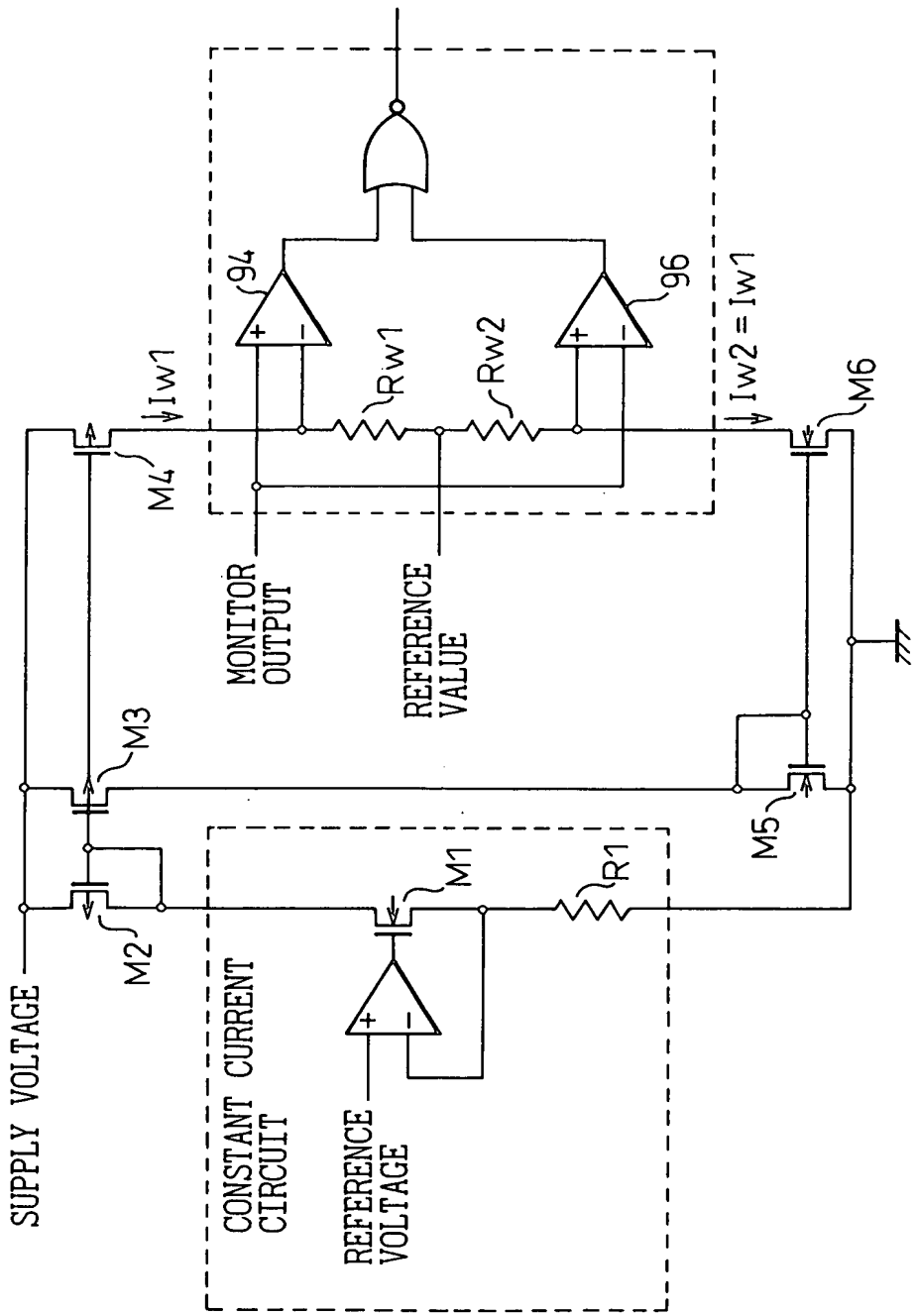

SUPPLY VOLTAGE
CONSTANT CURRENT CIRCUIT
REFERENCE VOLTAGE
M1
R1
M2
M3
M4
M5
M6
Iw1
Iw2 = Iw1
Rw1
Rw2
94
96
MONITOR OUTPUT
REFERENCE VALUE

Fig.30

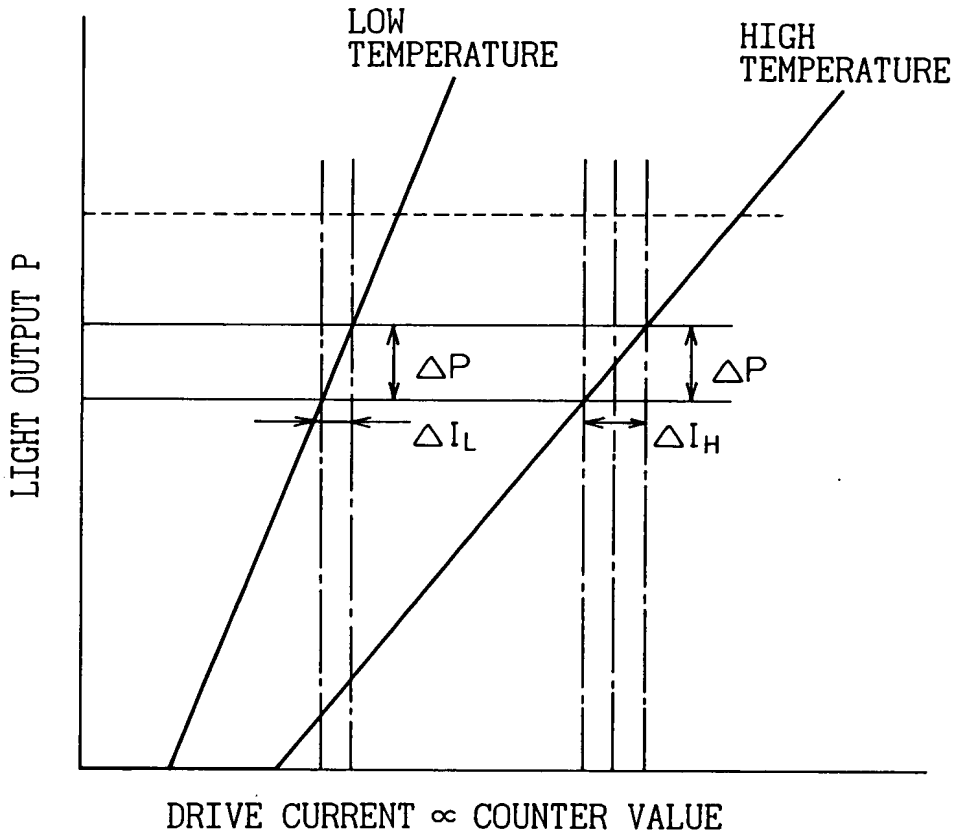

LOW
TEMPERATURE
HIGH
TEMPERATURE
LIGHT OUTPUT P
ΔP
ΔP
ΔI_L
ΔI_H
DRIVE CURRENT ∝ COUNTER VALUE

Fig.31

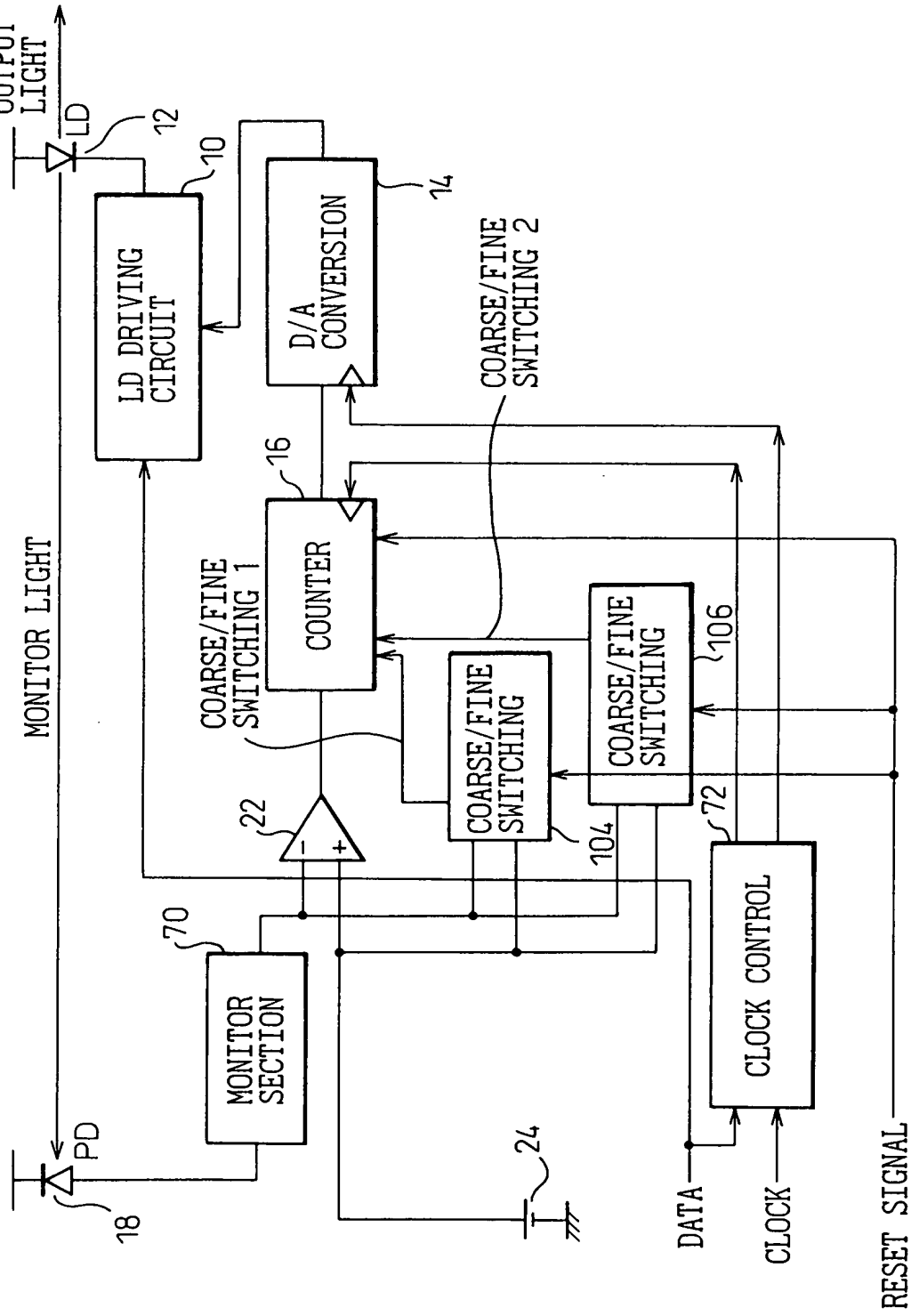

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
D/A CONVERSION
14
COARSE/FINE SWITCHING 2
16
COUNTER
COARSE/FINE SWITCHING 1
22
COARSE/FINE SWITCHING
104
COARSE/FINE SWITCHING
106
72
70
MONITOR SECTION
CLOCK CONTROL
MONITOR LIGHT
PD
18
24
DATA
CLOCK
RESET SIGNAL

Fig.32

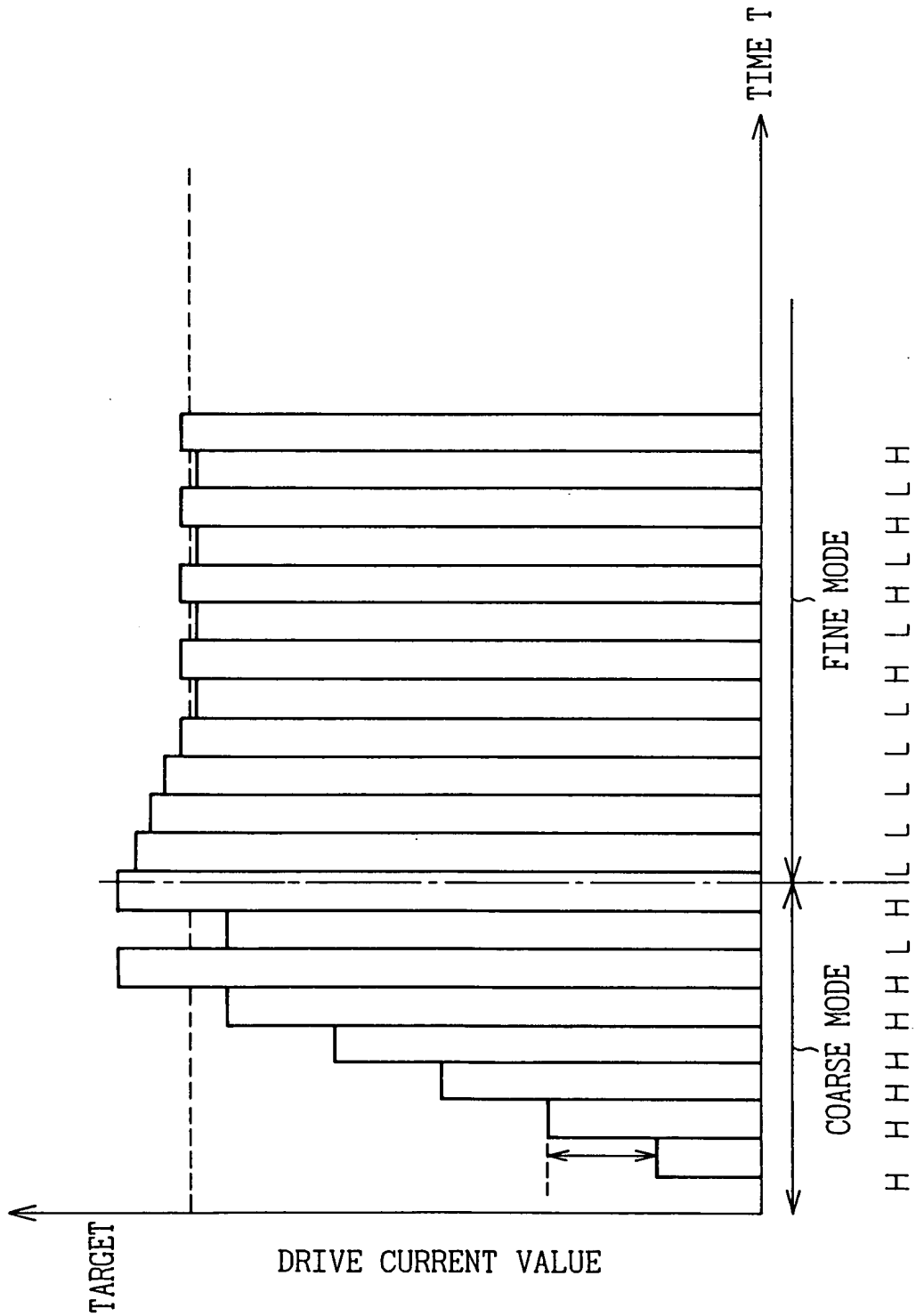

TIME T
FINE MODE
COARSE MODE
H H H H H H L H L L L L L H L H L H
TARGET
DRIVE CURRENT VALUE

Fig.33

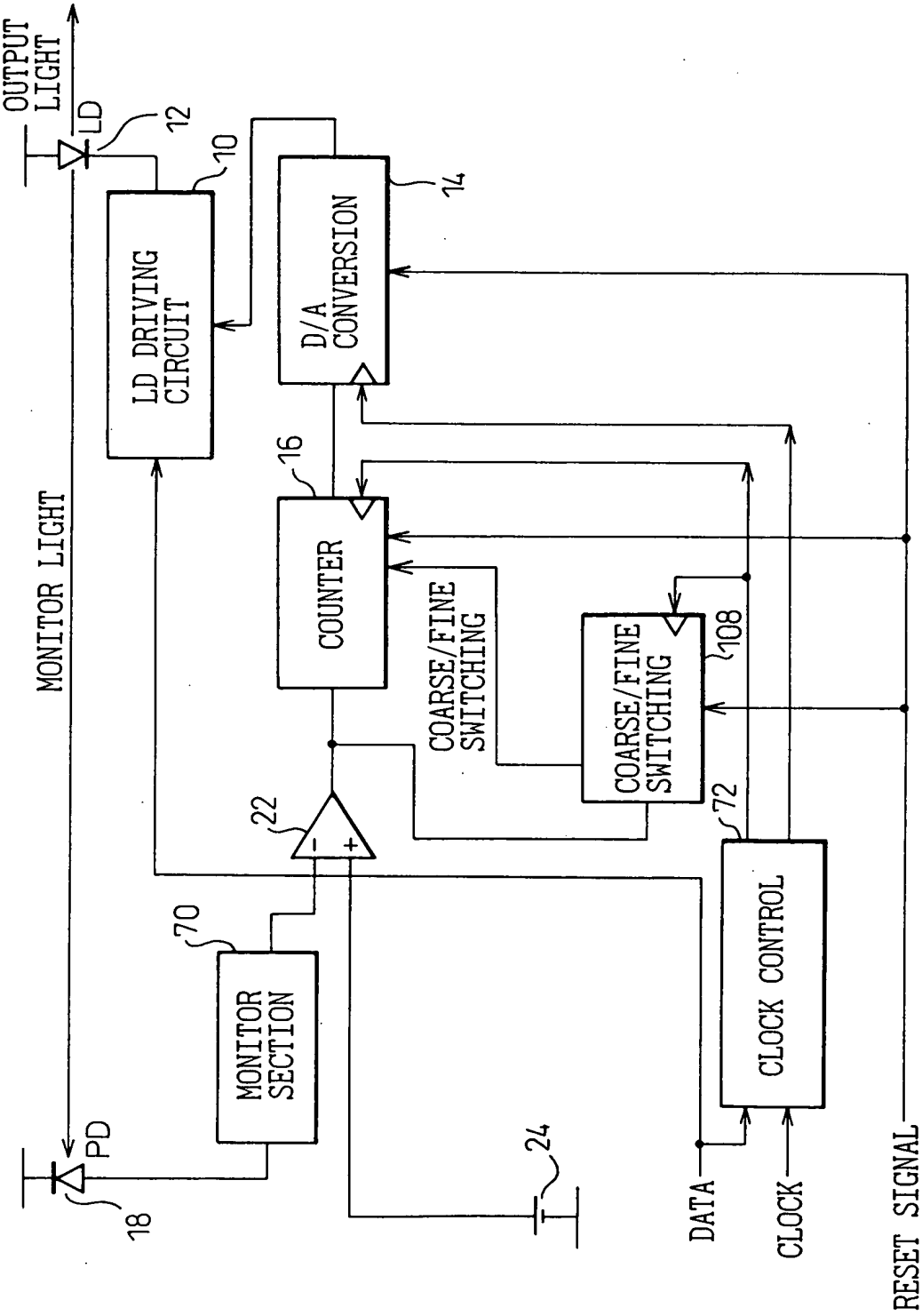

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
D/A CONVERSION
14
16
COUNTER
MONITOR LIGHT
COARSE/FINE SWITCHING
COARSE/FINE SWITCHING
108
22
72
70
MONITOR SECTION
CLOCK CONTROL
PD
18
24
DATA
CLOCK
RESET SIGNAL

Fig.34

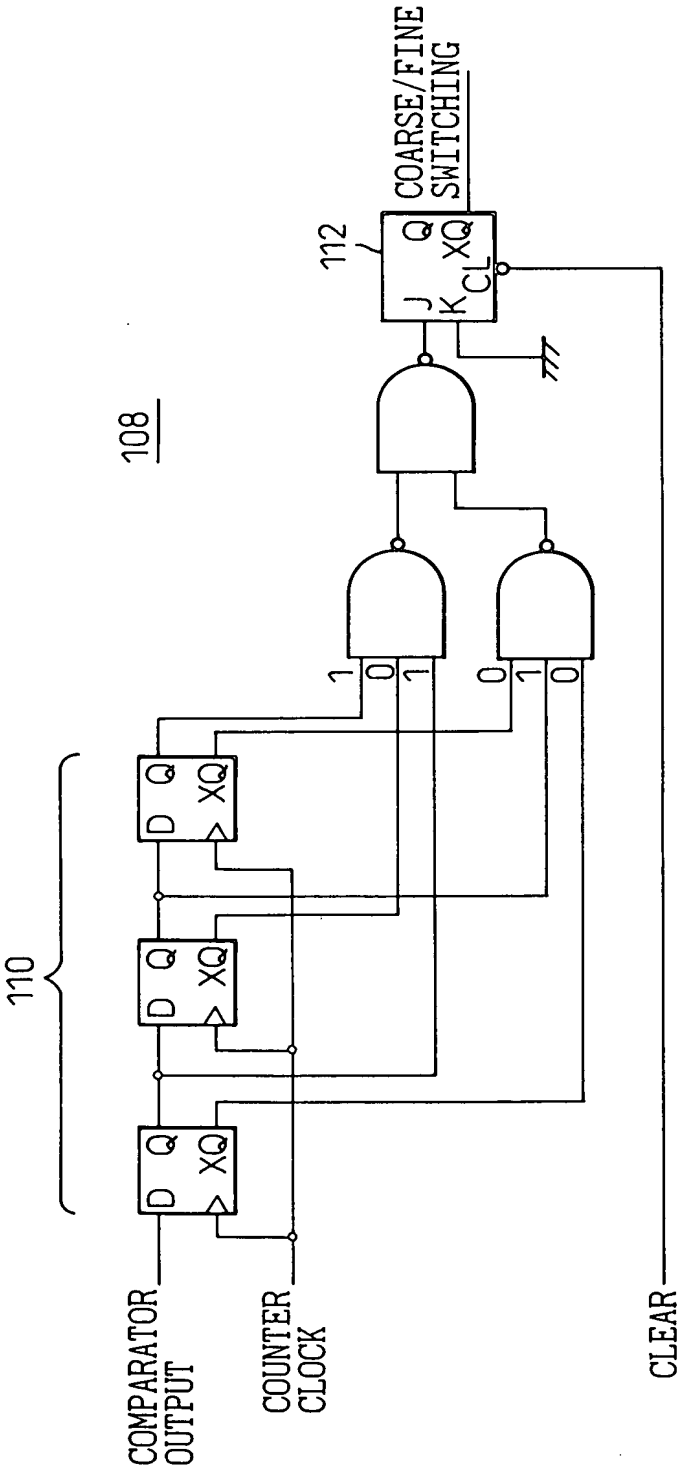

108
110
112
D Q
XQ
J Q
K XQ
CL
1
0
COMPARATOR OUTPUT
COUNTER CLOCK
COARSE/FINE SWITCHING
CLEAR

Fig.35

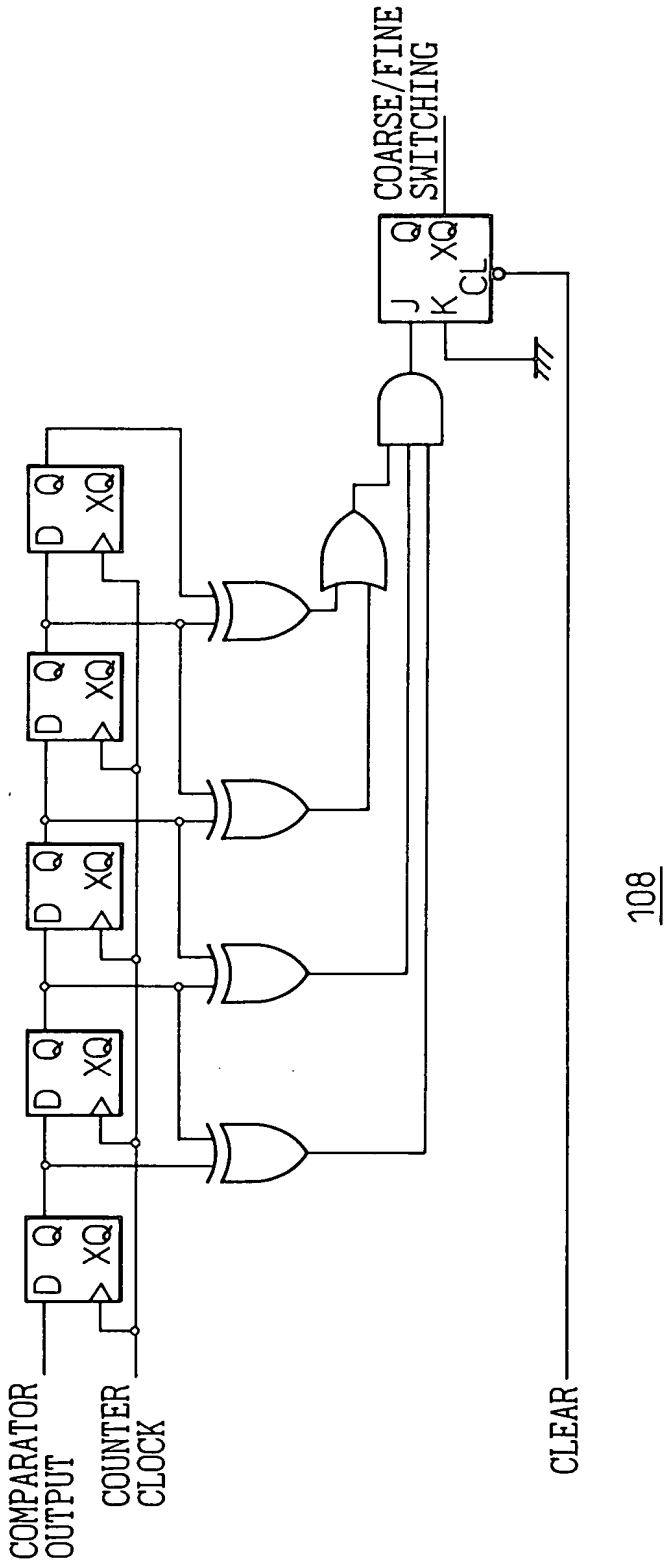

114
D Q
XQ
COMPARATOR OUTPUT
COUNTER CLOCK
J Q
K XQ
CL
COARSE/FINE SWITCHING
CLEAR
108

Fig.36

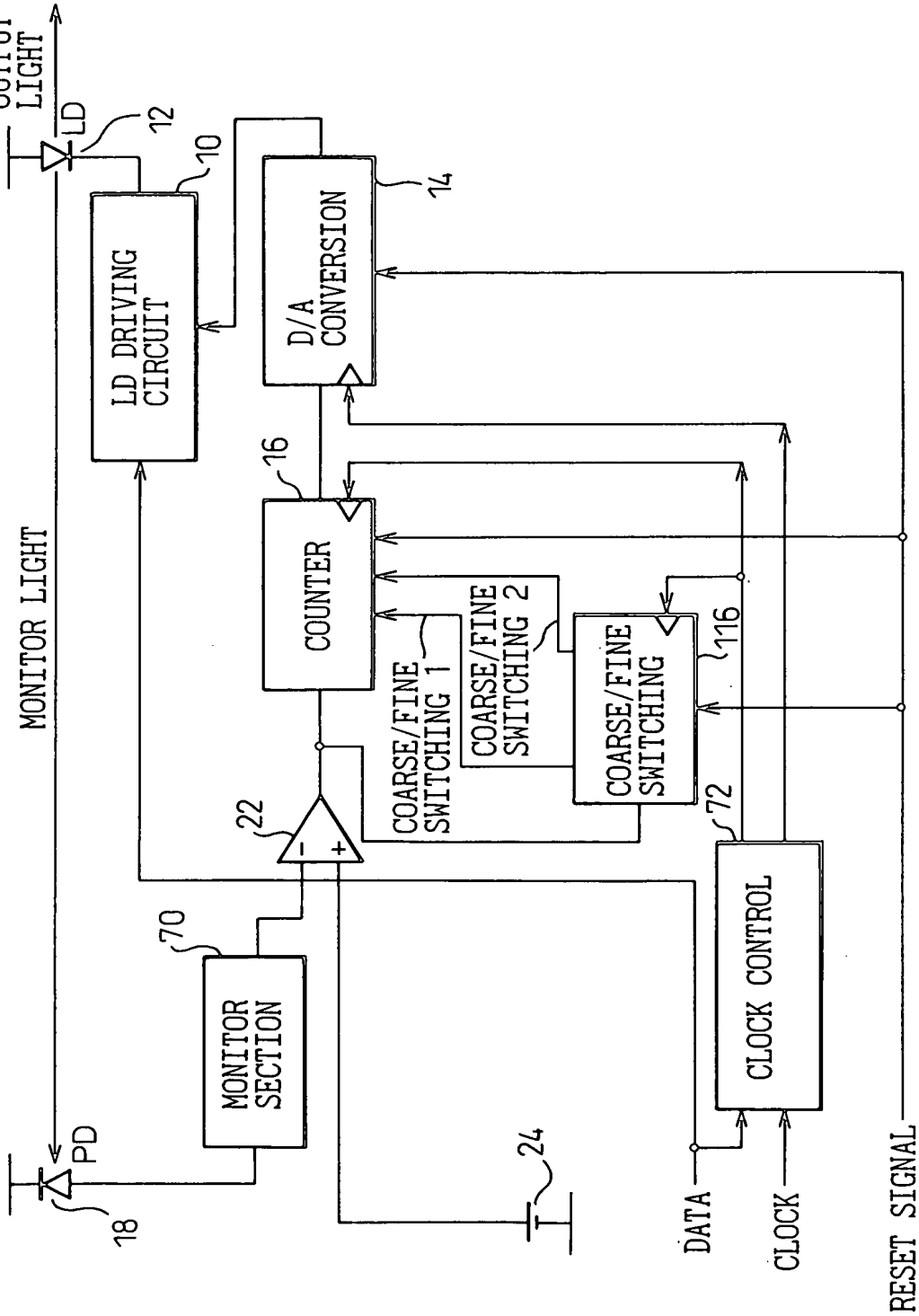

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
D/A CONVERSION
14
16
COUNTER
MONITOR LIGHT
COARSE/FINE SWITCHING 1
COARSE/FINE SWITCHING 2
COARSE/FINE SWITCHING
116
72
22
70
MONITOR SECTION
CLOCK CONTROL
PD
18
24
DATA
CLOCK
RESET SIGNAL

Fig.37

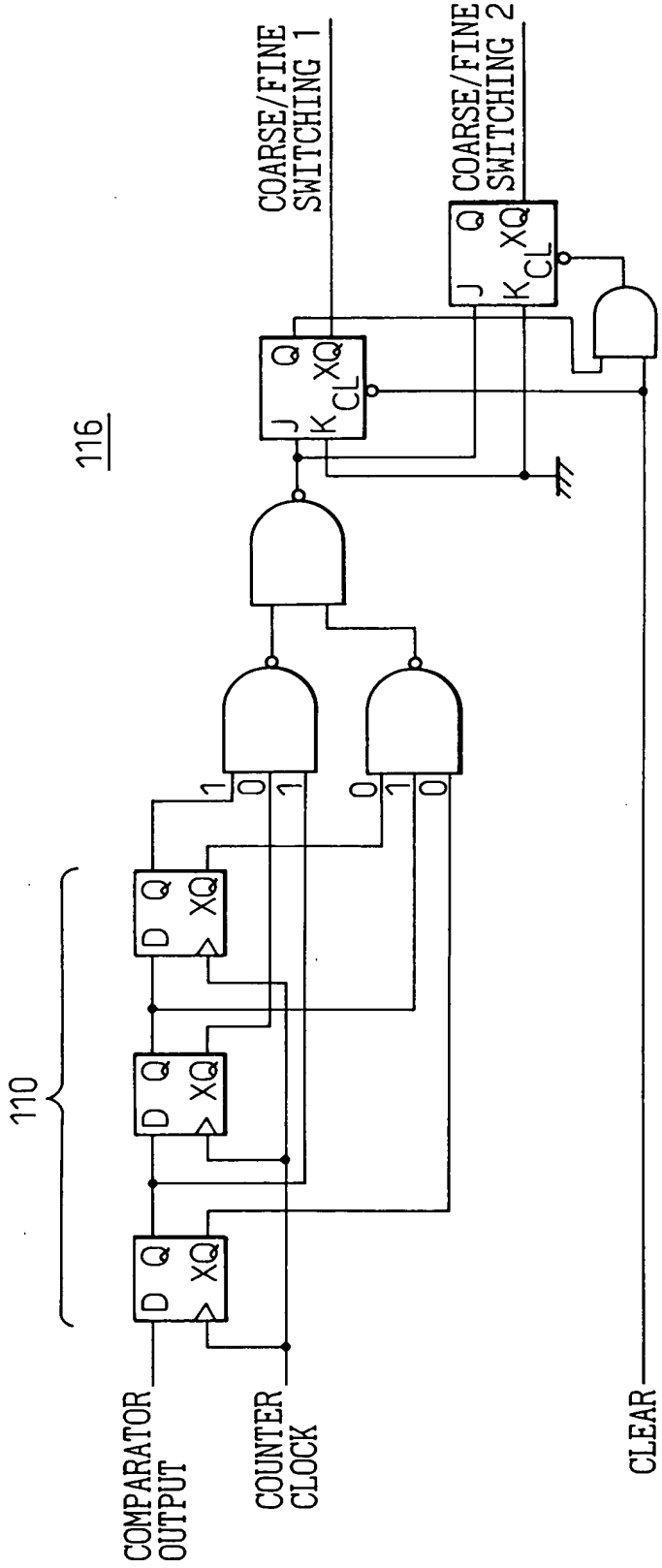

COARSE/FINE SWITCHING 1
COARSE/FINE SWITCHING 2
116
110
COMPARATOR OUTPUT
COUNTER CLOCK
CLEAR
D Q XQ
J K CL Q XQ
1 0

Fig.38

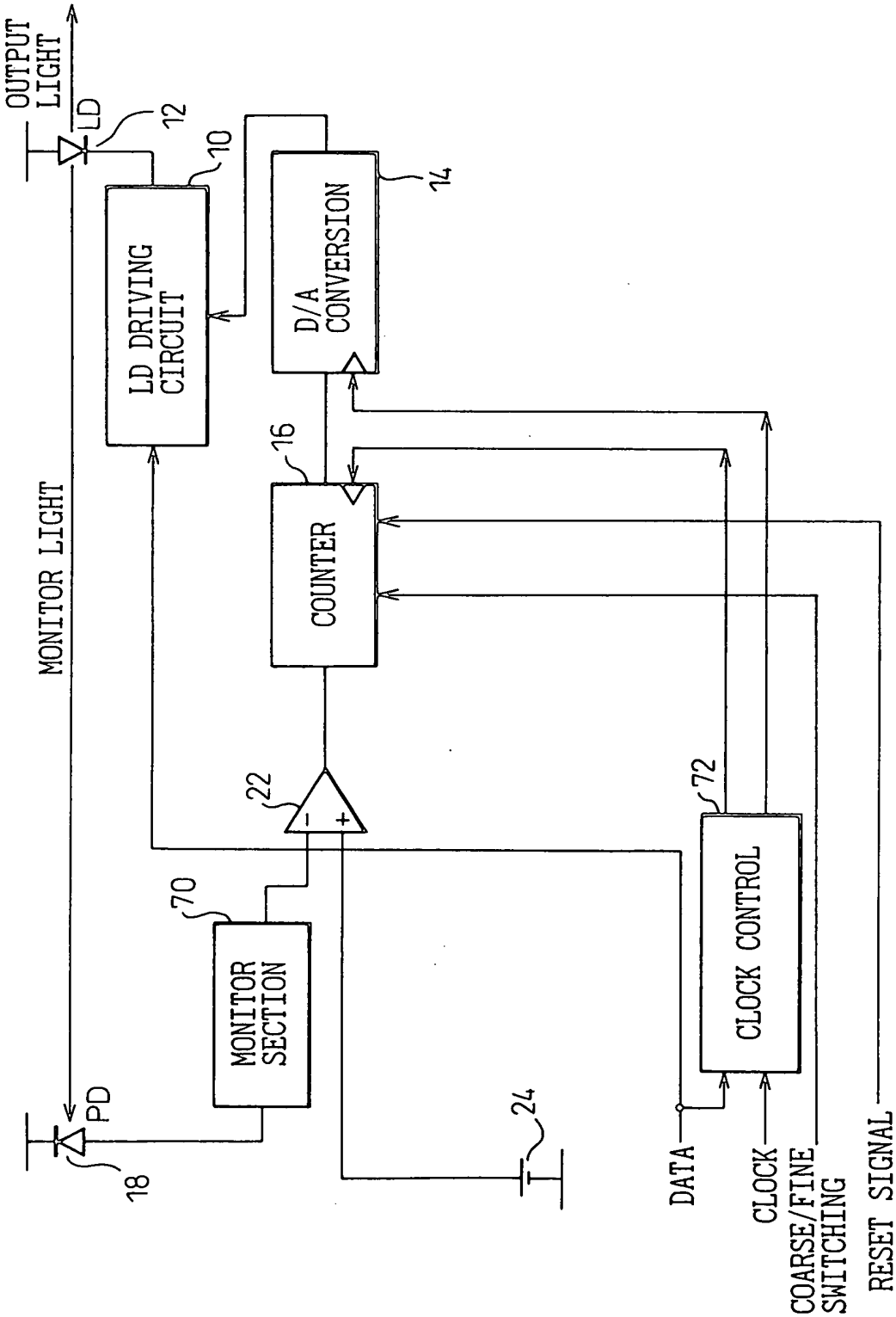

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
D/A CONVERSION
14
16
COUNTER
MONITOR LIGHT
22
72
CLOCK CONTROL
70
MONITOR SECTION
PD
18
24
DATA
CLOCK
COARSE/FINE SWITCHING
RESET SIGNAL

Fig.39

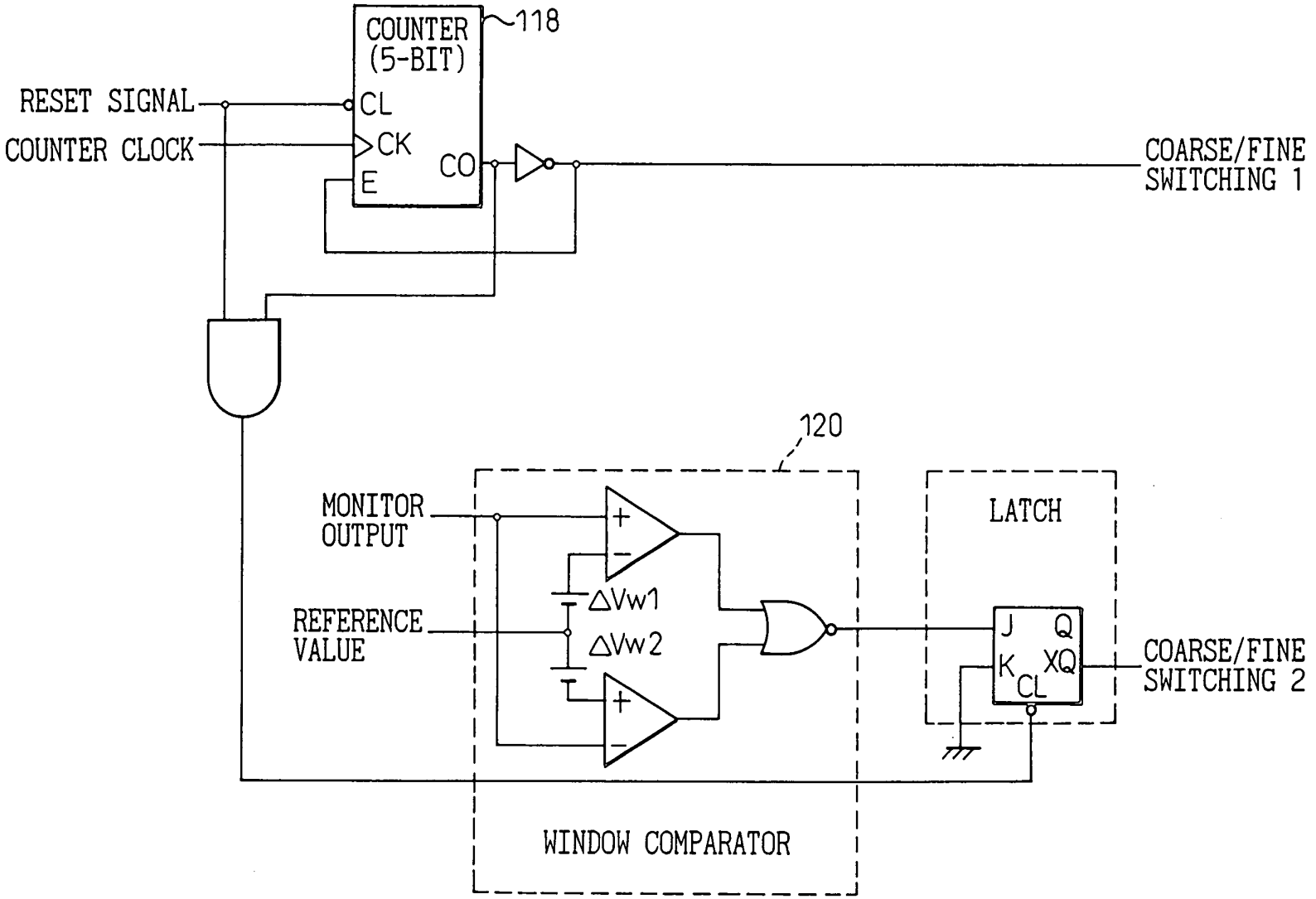

COUNTER
(5-BIT)
118
RESET SIGNAL
COUNTER CLOCK
CL
CK
E
CO
COARSE/FINE
SWITCHING 1
120
MONITOR
OUTPUT
REFERENCE
VALUE
ΔVw1
ΔVw2
LATCH
J
Q
K
CL
XQ
COARSE/FINE
SWITCHING 2
WINDOW COMPARATOR

Fig.40

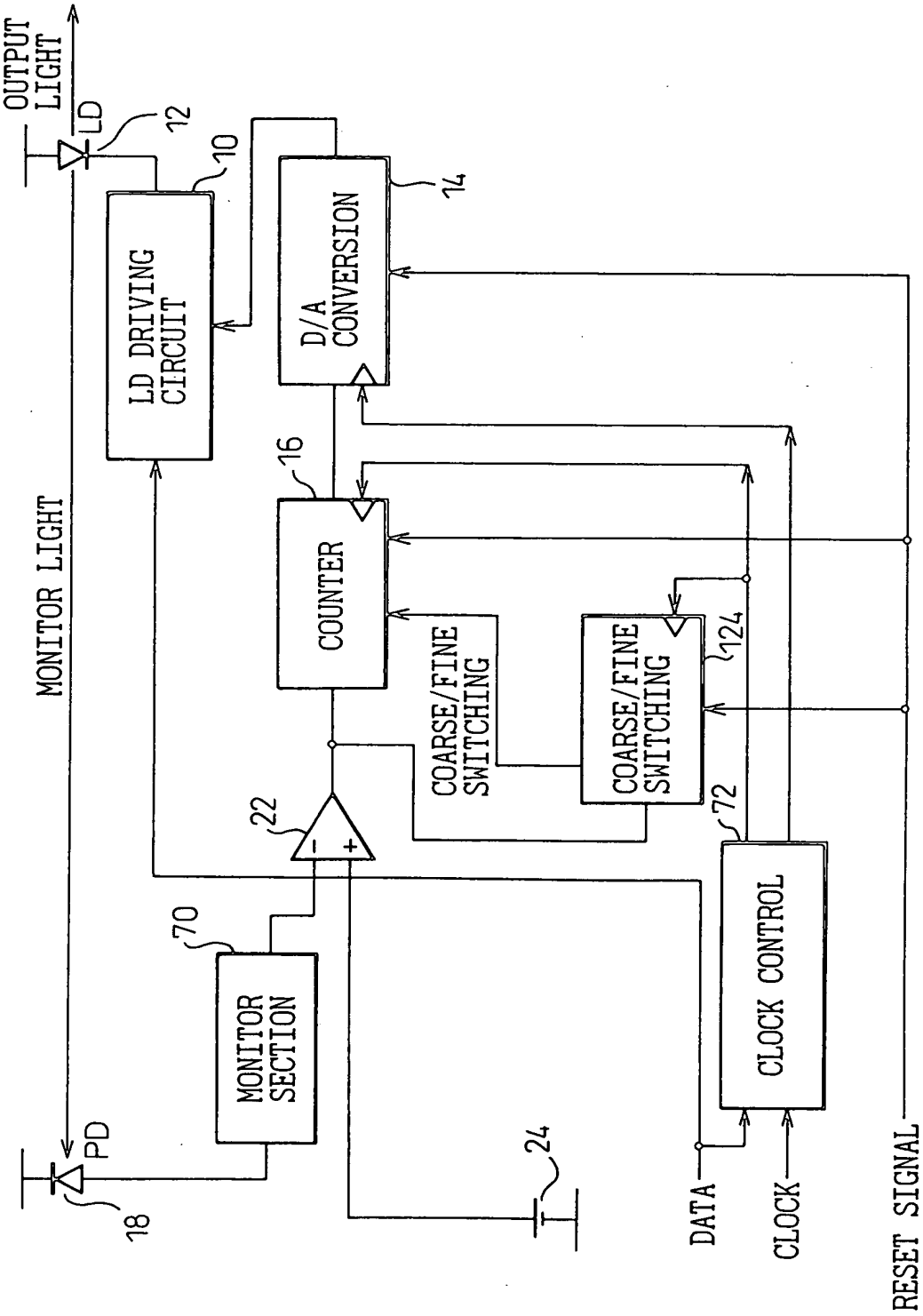

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
D/A CONVERSION
14
16
COUNTER
MONITOR LIGHT
COARSE/FINE SWITCHING
COARSE/FINE SWITCHING
124
22
72
70
MONITOR SECTION
CLOCK CONTROL
PD
18
24
DATA
CLOCK
RESET SIGNAL

Fig. 41

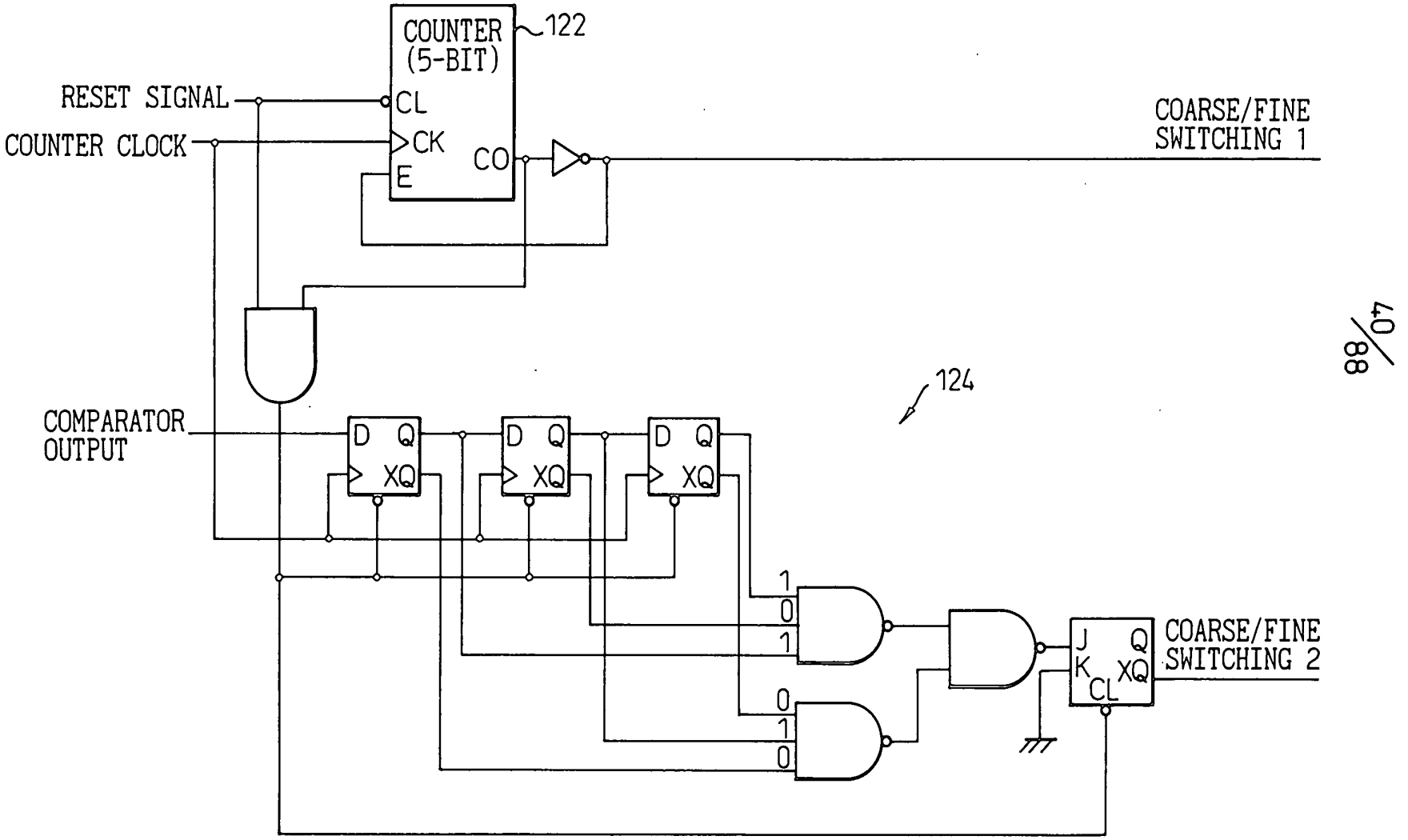

COUNTER
(5-BIT)
122
RESET SIGNAL
COUNTER CLOCK
CL
CK
E
CO
COARSE/FINE
SWITCHING 1
124
COMPARATOR
OUTPUT
D Q
XQ
1
0
1
0
1
0
J Q
K XQ
CL
COARSE/FINE
SWITCHING 2

Fig. 42

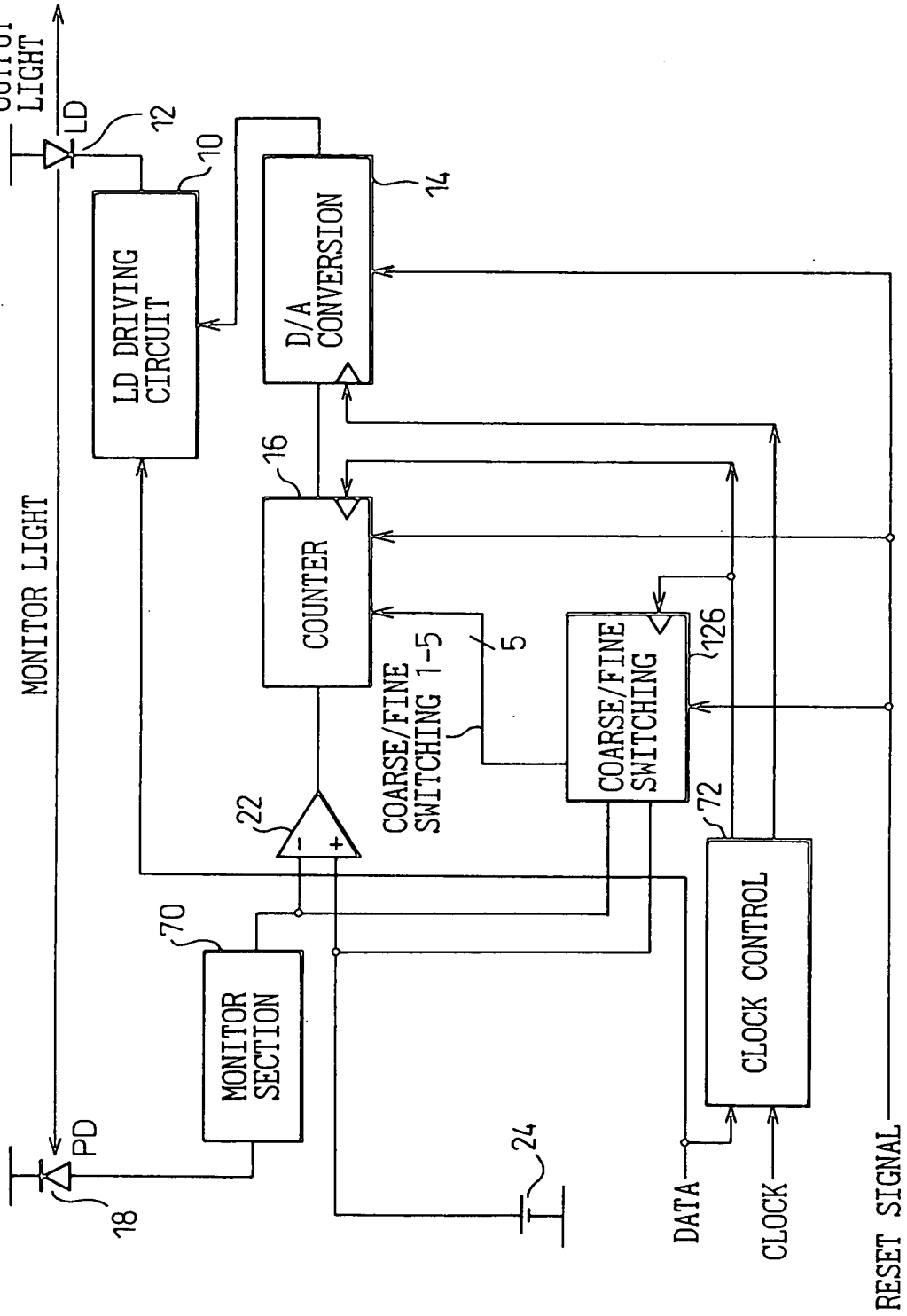

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
D/A CONVERSION
14
16
COUNTER
MONITOR LIGHT
COARSE/FINE SWITCHING 1-5
5
COARSE/FINE SWITCHING
126
22
72
70
MONITOR SECTION
CLOCK CONTROL
PD
18
24
DATA
CLOCK
RESET SIGNAL

Fig. 43

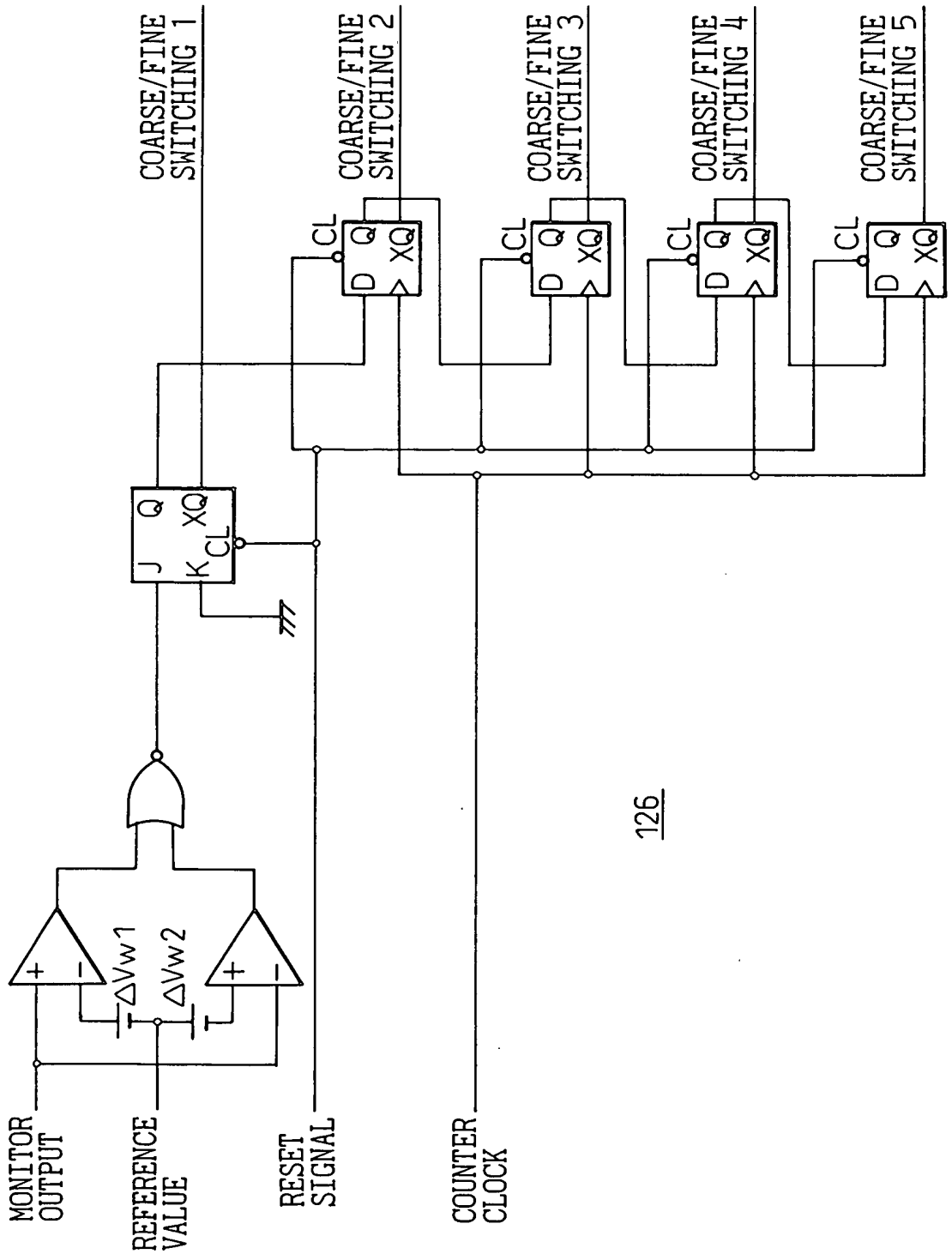

COARSE/FINE SWITCHING 1
COARSE/FINE SWITCHING 2
COARSE/FINE SWITCHING 3
COARSE/FINE SWITCHING 4
COARSE/FINE SWITCHING 5
CL
D
Q
XQ
J
K
ΔVw1
ΔVw2
MONITOR OUTPUT
REFERENCE VALUE
RESET SIGNAL
COUNTER CLOCK
126

Fig. 44

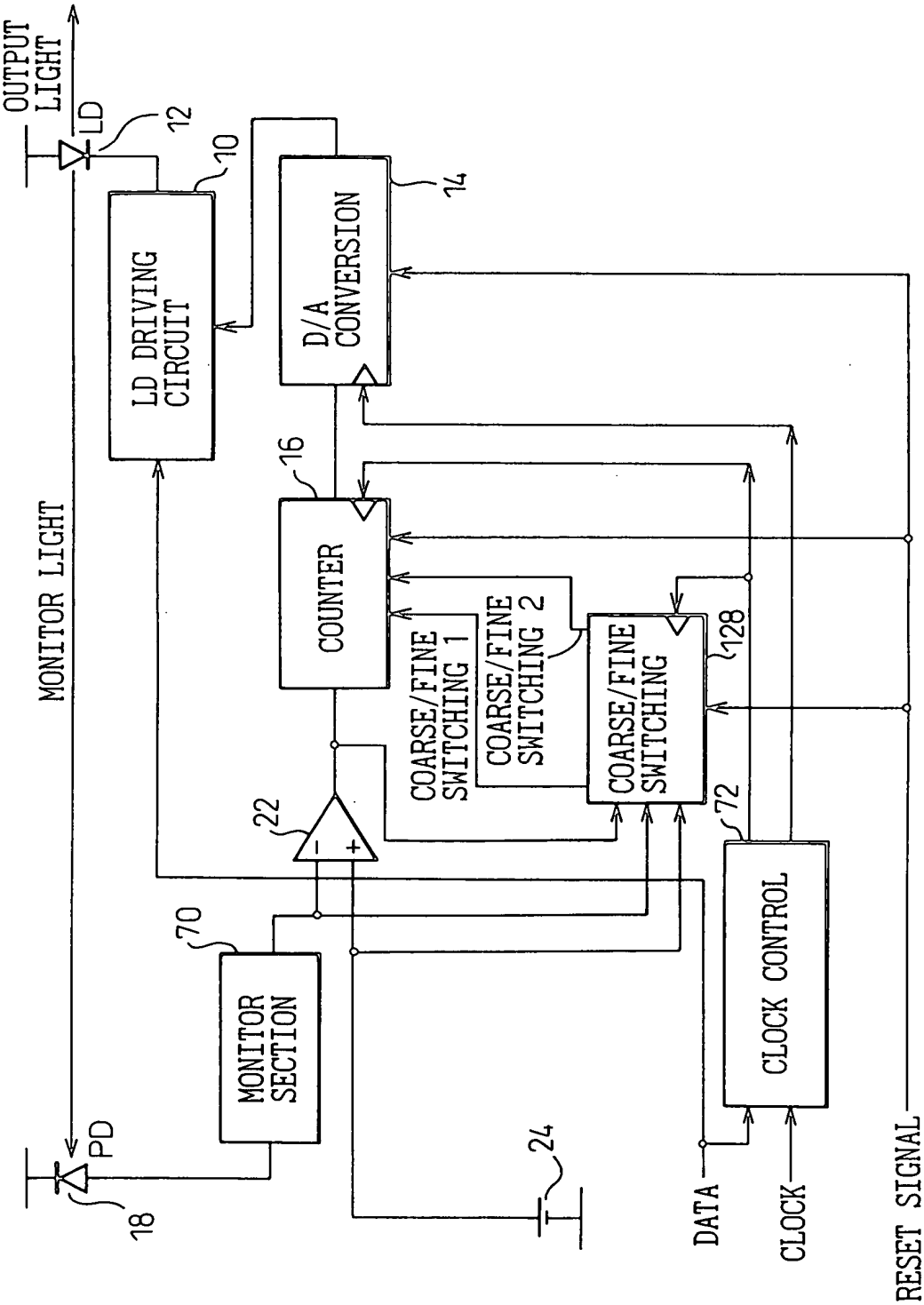

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
14
D/A CONVERSION
16
COUNTER
MONITOR LIGHT
COARSE/FINE SWITCHING 1
COARSE/FINE SWITCHING 2
COARSE/FINE SWITCHING
128
72
22
70
MONITOR SECTION
CLOCK CONTROL
PD
18
24
DATA
CLOCK
RESET SIGNAL

Fig.45

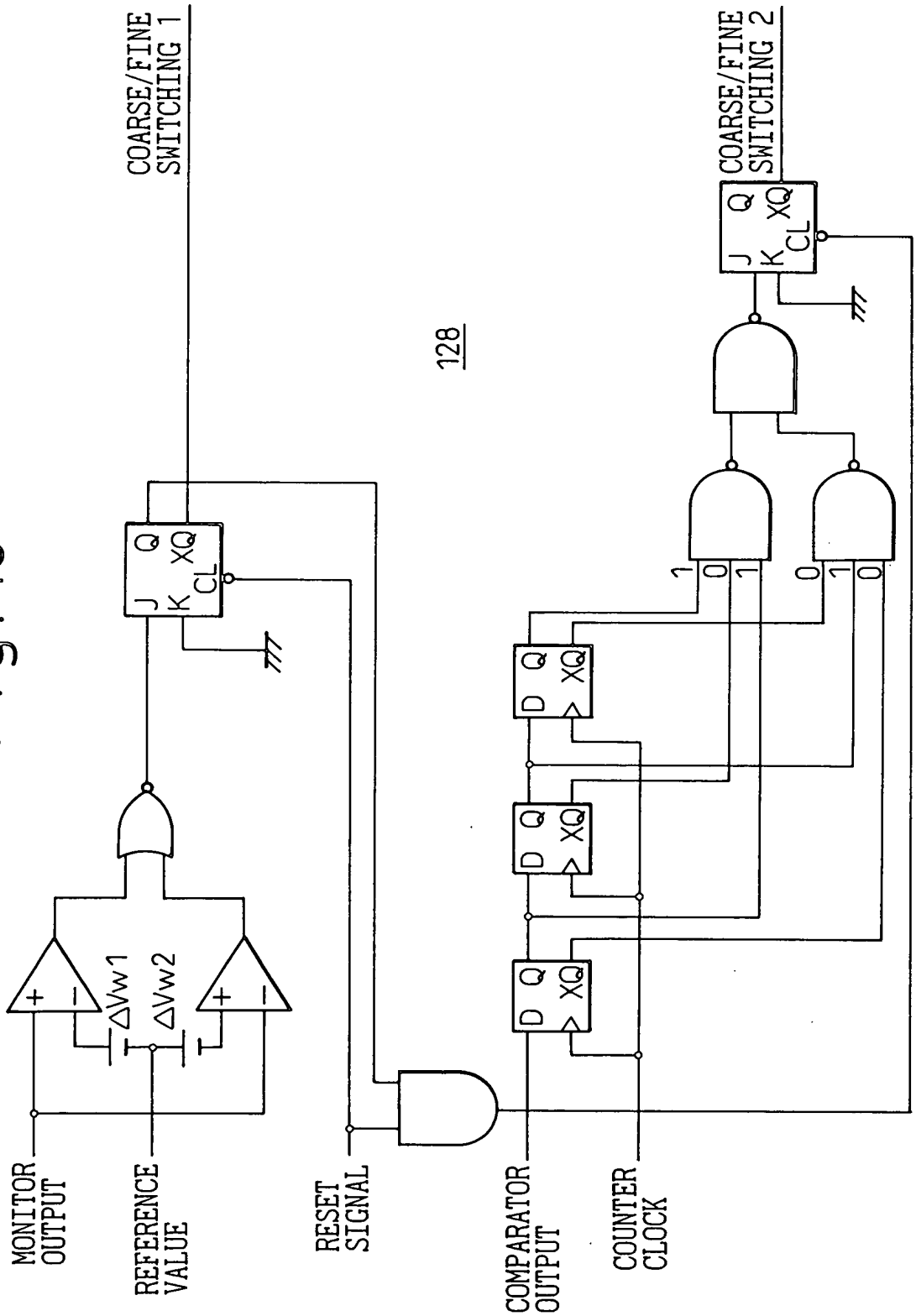

128
COARSE/FINE SWITCHING 1
COARSE/FINE SWITCHING 2
MONITOR OUTPUT
REFERENCE VALUE
RESET SIGNAL
COMPARATOR OUTPUT
COUNTER CLOCK
ΔVw1
ΔVw2
J
K
Q
XQ
CL
D
1
0

Fig.46

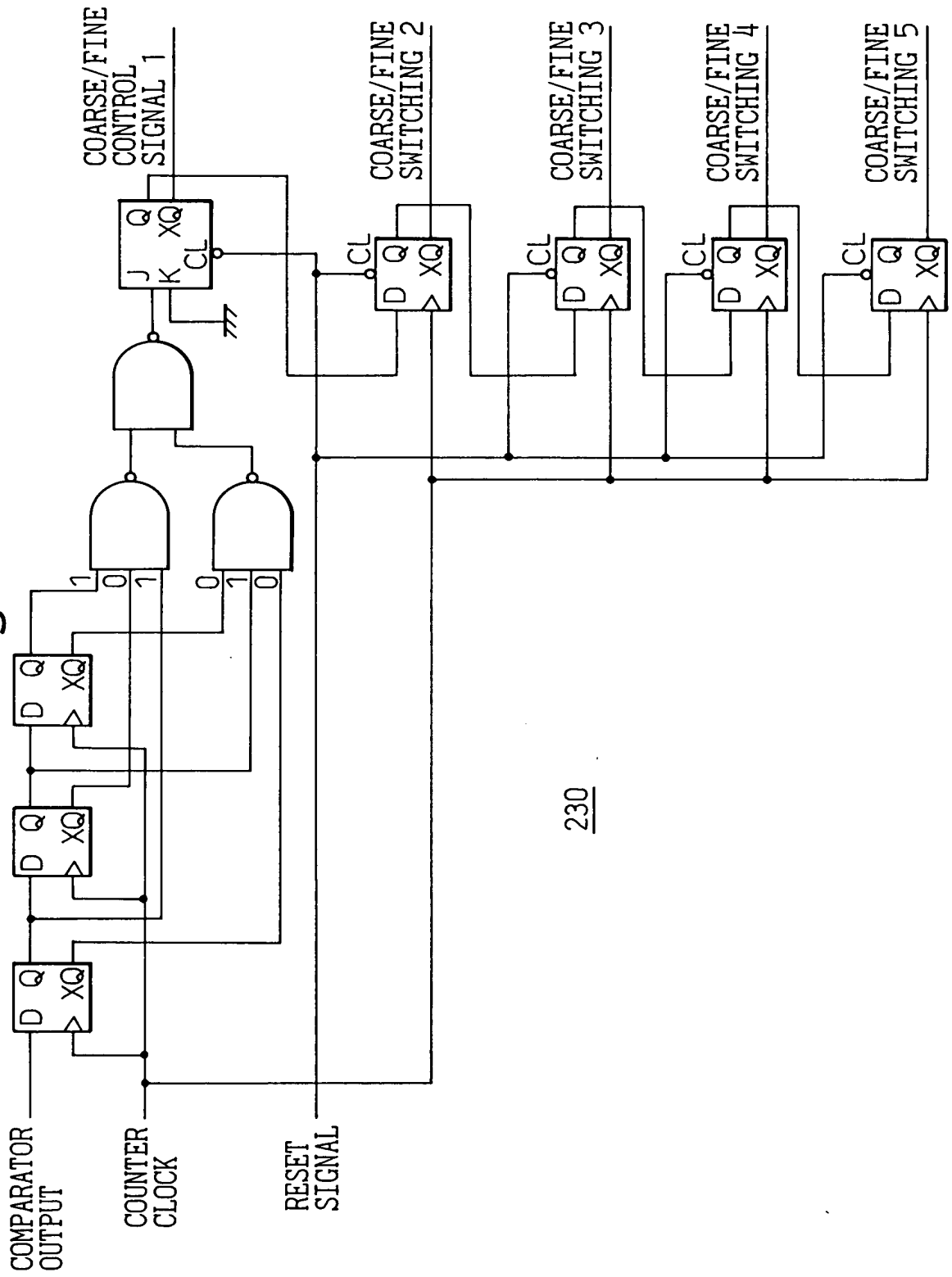

COARSE/FINE CONTROL SIGNAL 1
COARSE/FINE SWITCHING 2
COARSE/FINE SWITCHING 3
COARSE/FINE SWITCHING 4
COARSE/FINE SWITCHING 5
COMPARATOR OUTPUT
COUNTER CLOCK
RESET SIGNAL
230

Fig.47

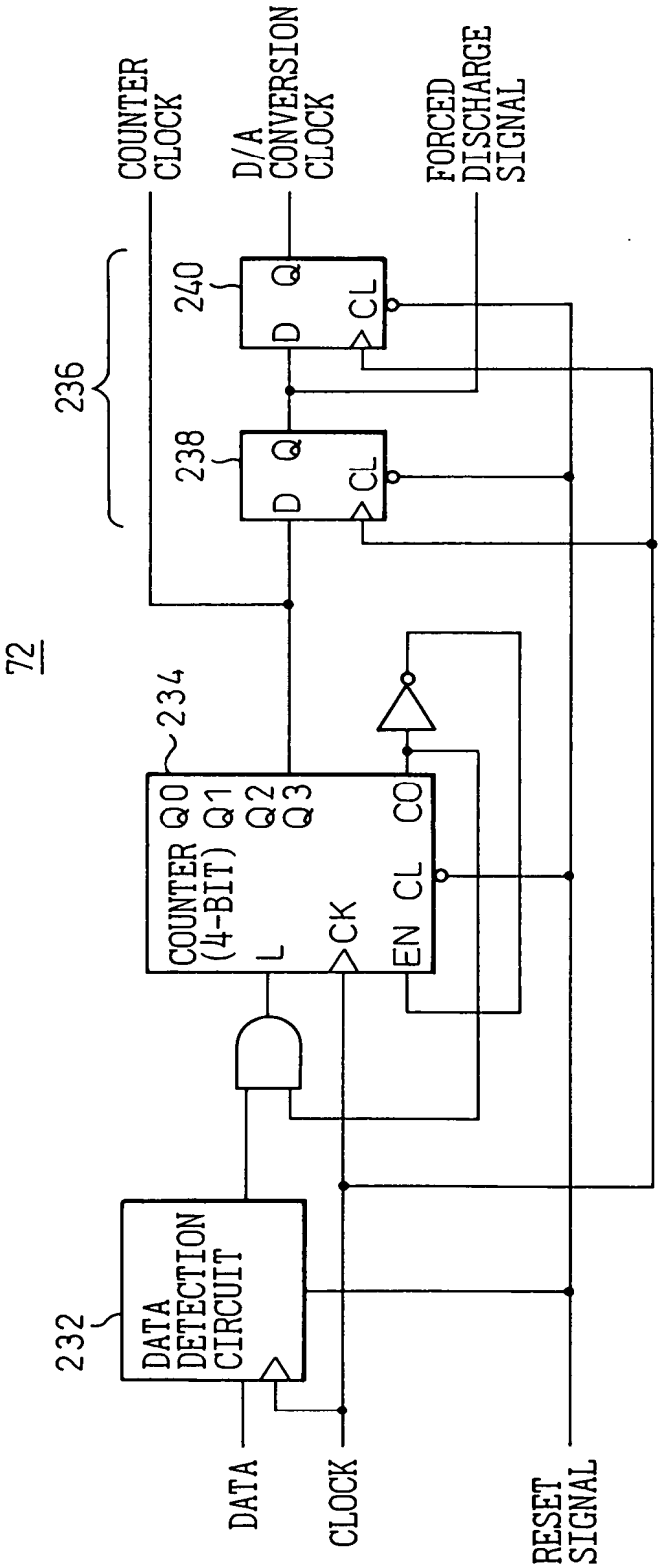

72
232
DATA DETECTION CIRCUIT
234
COUNTER (4-BIT)
Q0
Q1
Q2
Q3
CO
L
CK
EN
CL
236
238
240
D
Q
CL
COUNTER CLOCK
D/A CONVERSION CLOCK
FORCED DISCHARGE SIGNAL
DATA
CLOCK
RESET SIGNAL

Fig.48

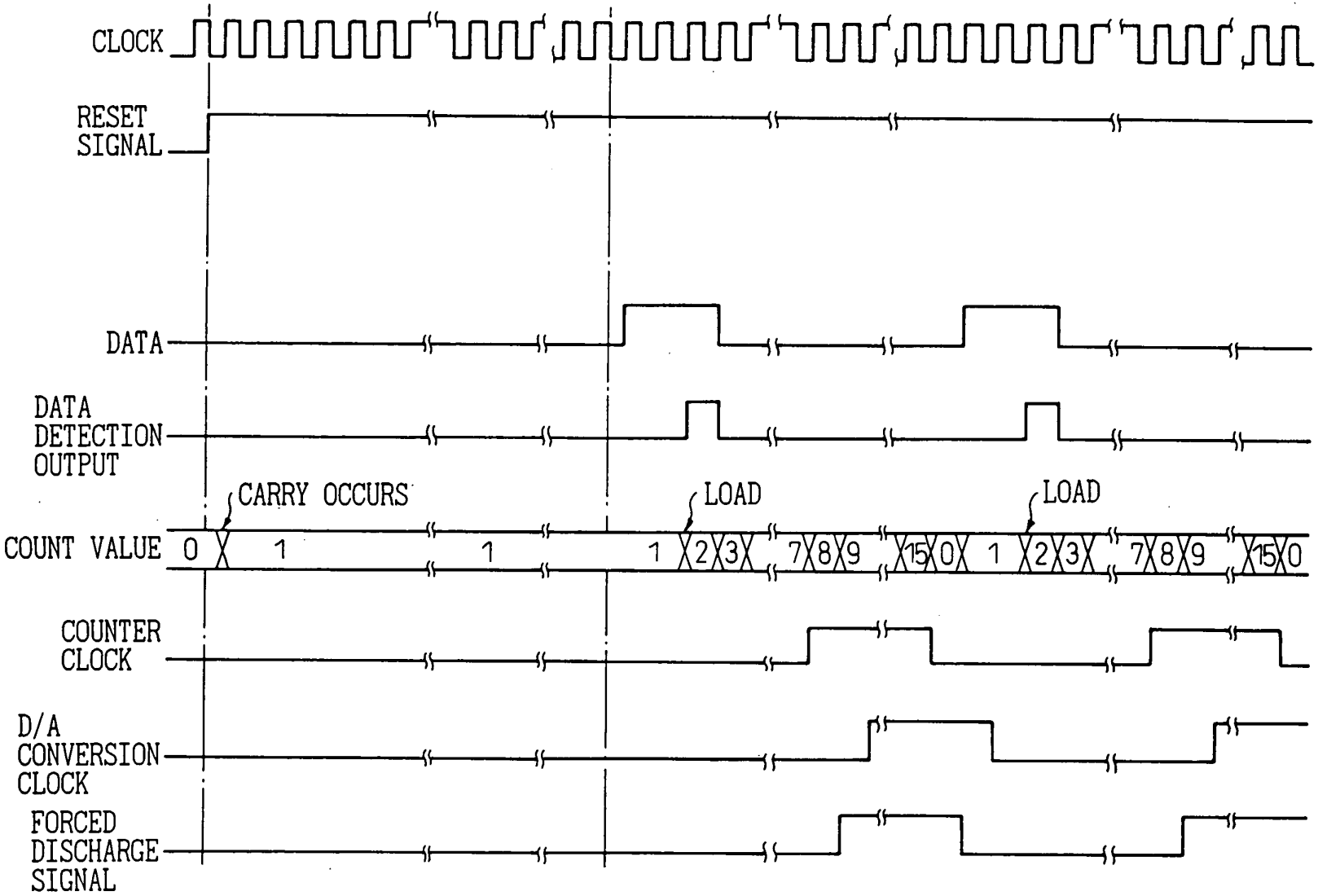

CLOCK
RESET SIGNAL
DATA
DATA DETECTION OUTPUT
CARRY OCCURS
LOAD
LOAD
COUNT VALUE
0 1 1 1 2 3 7 8 9 15 0 1 2 3 7 8 9 15 0
COUNTER CLOCK
D/A CONVERSION CLOCK
FORCED DISCHARGE SIGNAL

Fig.49

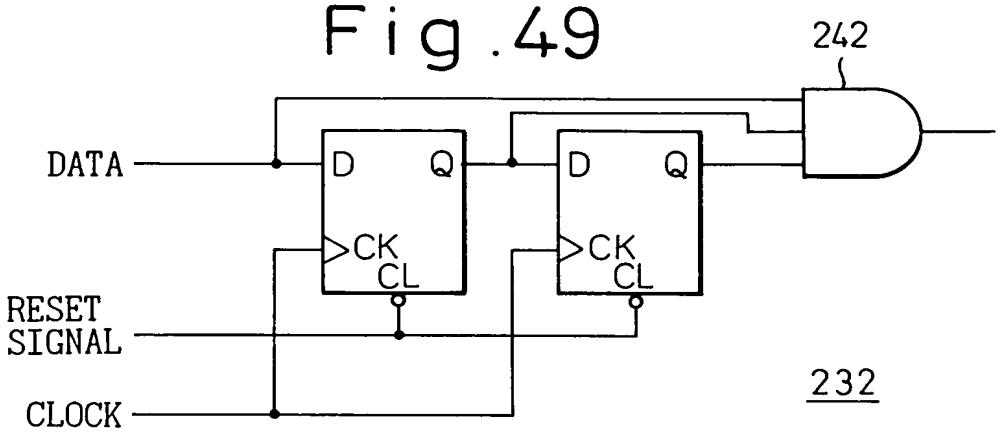

242
DATA
D
Q
D
Q
CK
CL
CK
CL
RESET
SIGNAL
CLOCK
232

Fig.50

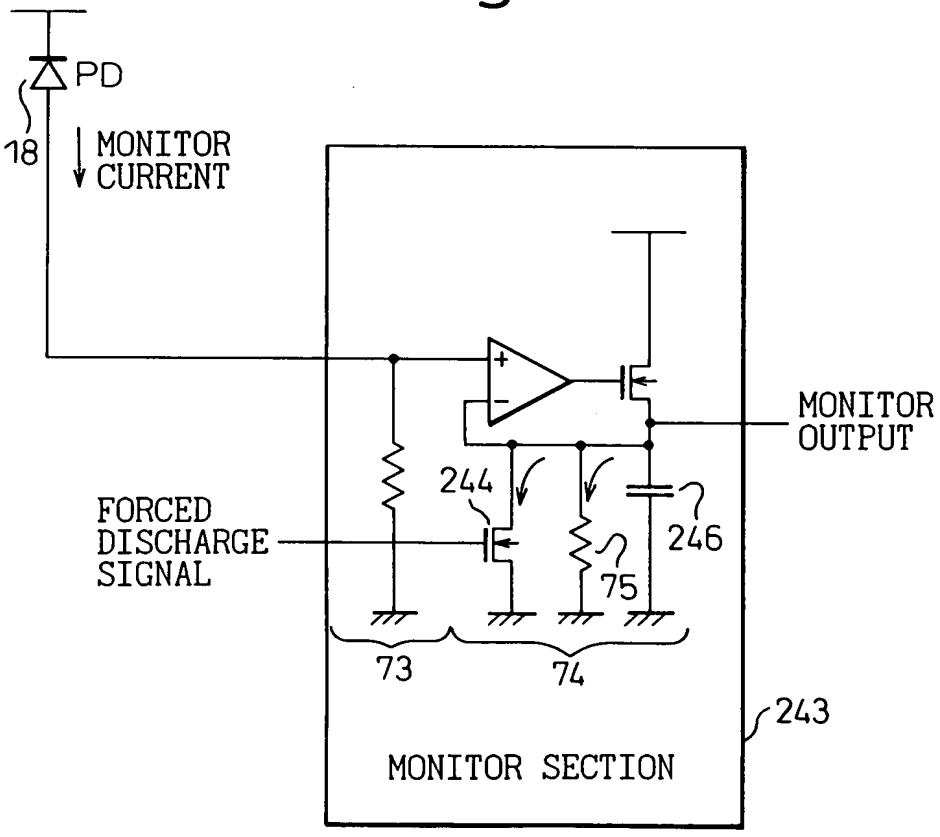

PD
18
MONITOR
CURRENT
MONITOR
OUTPUT
244
246
FORCED
DISCHARGE
SIGNAL
75
73
74
243
MONITOR SECTION

Fig.51

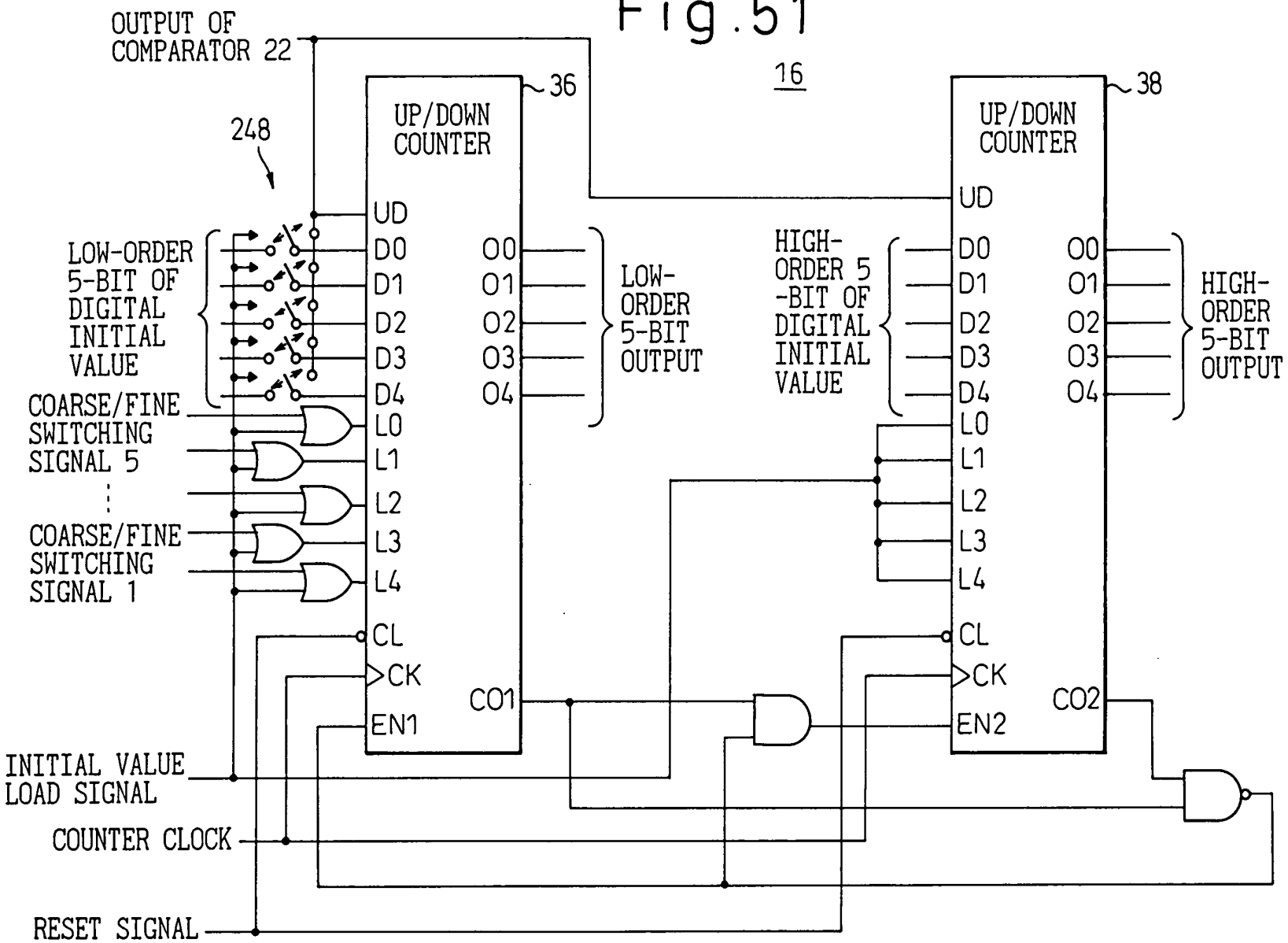

16
OUTPUT OF COMPARATOR 22
248
36
UP/DOWN COUNTER
38
UP/DOWN COUNTER
UD
D0
D1
D2
D3
D4
O0
O1
O2
O3
O4
LOW-ORDER 5-BIT OF DIGITAL INITIAL VALUE
LOW-ORDER 5-BIT OUTPUT
HIGH-ORDER 5-BIT OF DIGITAL INITIAL VALUE
HIGH-ORDER 5-BIT OUTPUT
COARSE/FINE SWITCHING SIGNAL 5
COARSE/FINE SWITCHING SIGNAL 1
L0
L1
L2
L3
L4
CL
CK
EN1
EN2
CO1
CO2
INITIAL VALUE LOAD SIGNAL
COUNTER CLOCK
RESET SIGNAL

Fig.52

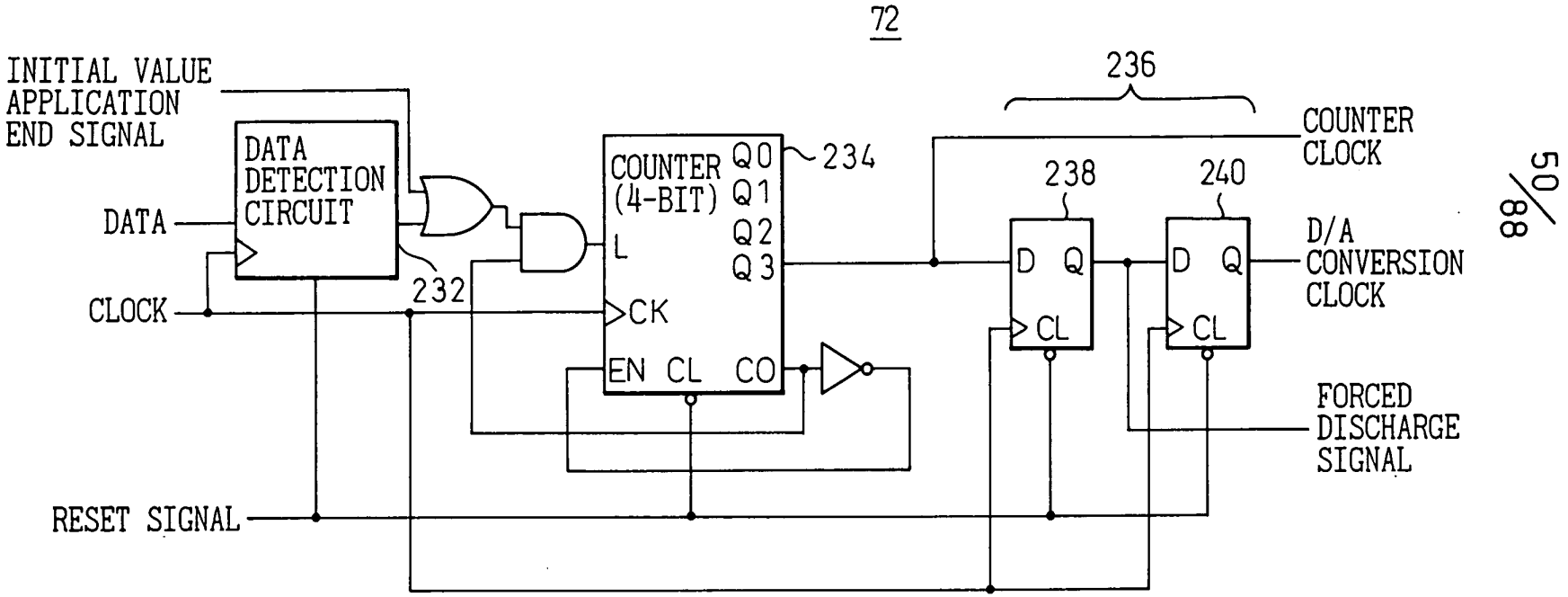

72
INITIAL VALUE APPLICATION END SIGNAL
DATA
CLOCK
DATA DETECTION CIRCUIT
232
COUNTER (4-BIT)
Q0
Q1
Q2
Q3
234
L
CK
EN CL CO
236
238
240
D Q
CL
COUNTER CLOCK
D/A CONVERSION CLOCK
FORCED DISCHARGE SIGNAL
RESET SIGNAL

Fig.53

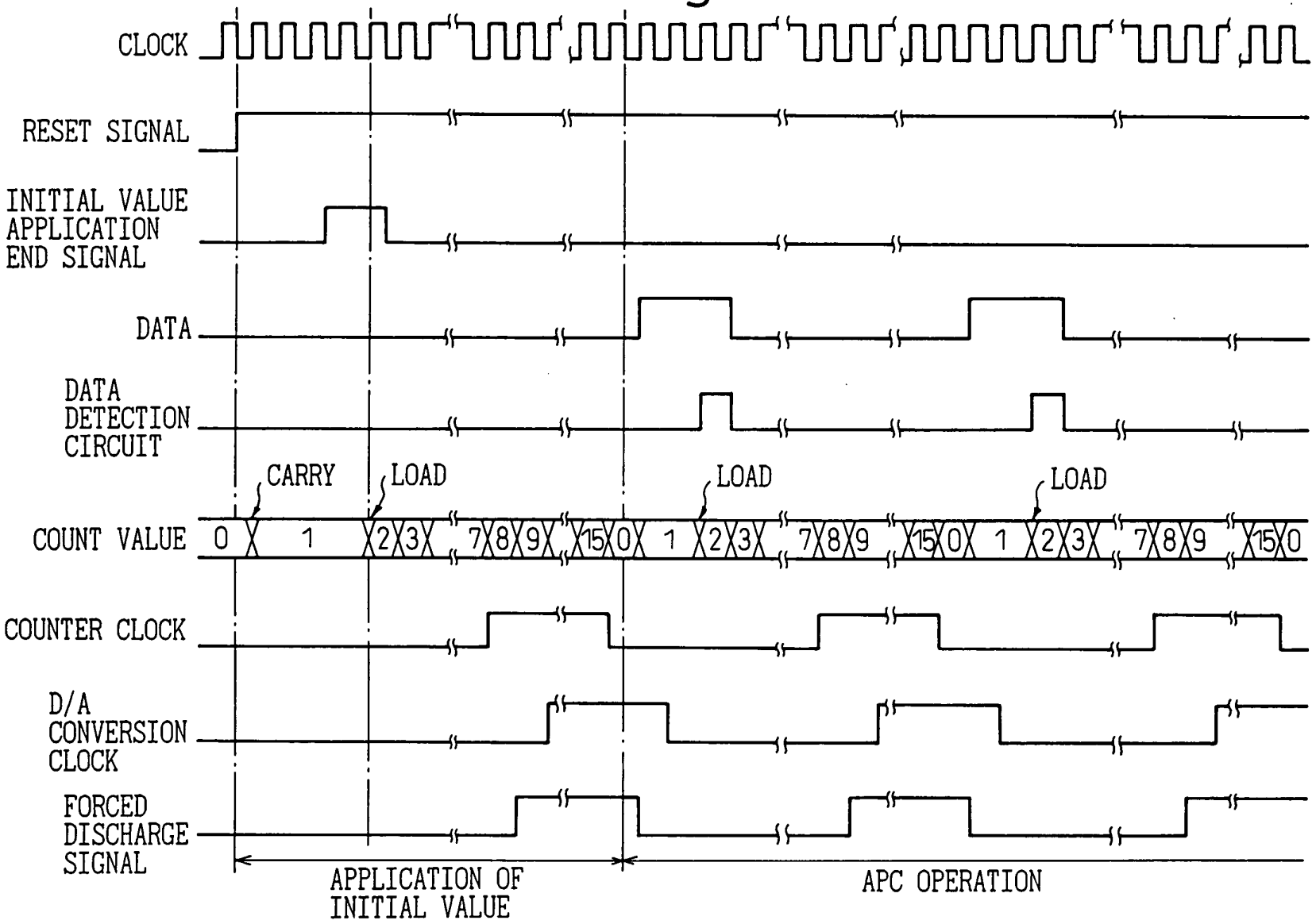

CLOCK
RESET SIGNAL
INITIAL VALUE APPLICATION END SIGNAL
DATA
DATA DETECTION CIRCUIT
CARRY
LOAD
LOAD
LOAD
COUNT VALUE
0 1 2 3 7 8 9 15 0 1 2 3 7 8 9 15 0 1 2 3 7 8 9 15 0
COUNTER CLOCK
D/A CONVERSION CLOCK
FORCED DISCHARGE SIGNAL
APPLICATION OF INITIAL VALUE
APC OPERATION

Fig. 54

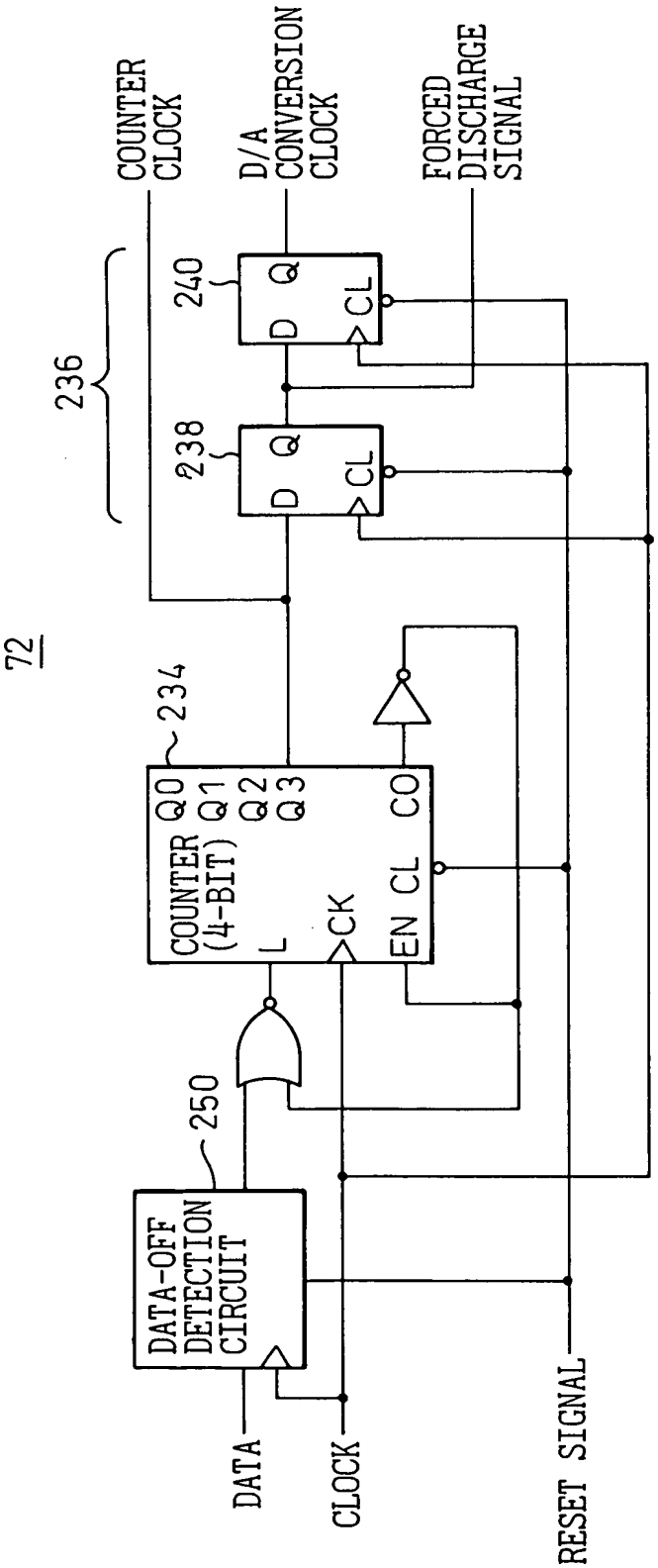

72
COUNTER CLOCK
D/A CONVERSION CLOCK
FORCED DISCHARGE SIGNAL
236
240
238
D Q
CL
234
COUNTER (4-BIT)
Q0 Q1 Q2 Q3
CO
L
CK
EN CL
250
DATA-OFF DETECTION CIRCUIT
DATA
CLOCK
RESET SIGNAL

Fig.55

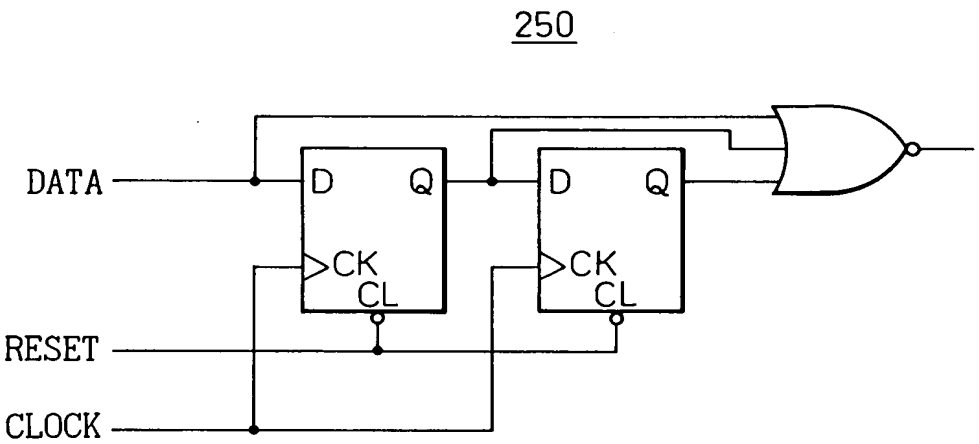


Fig.56

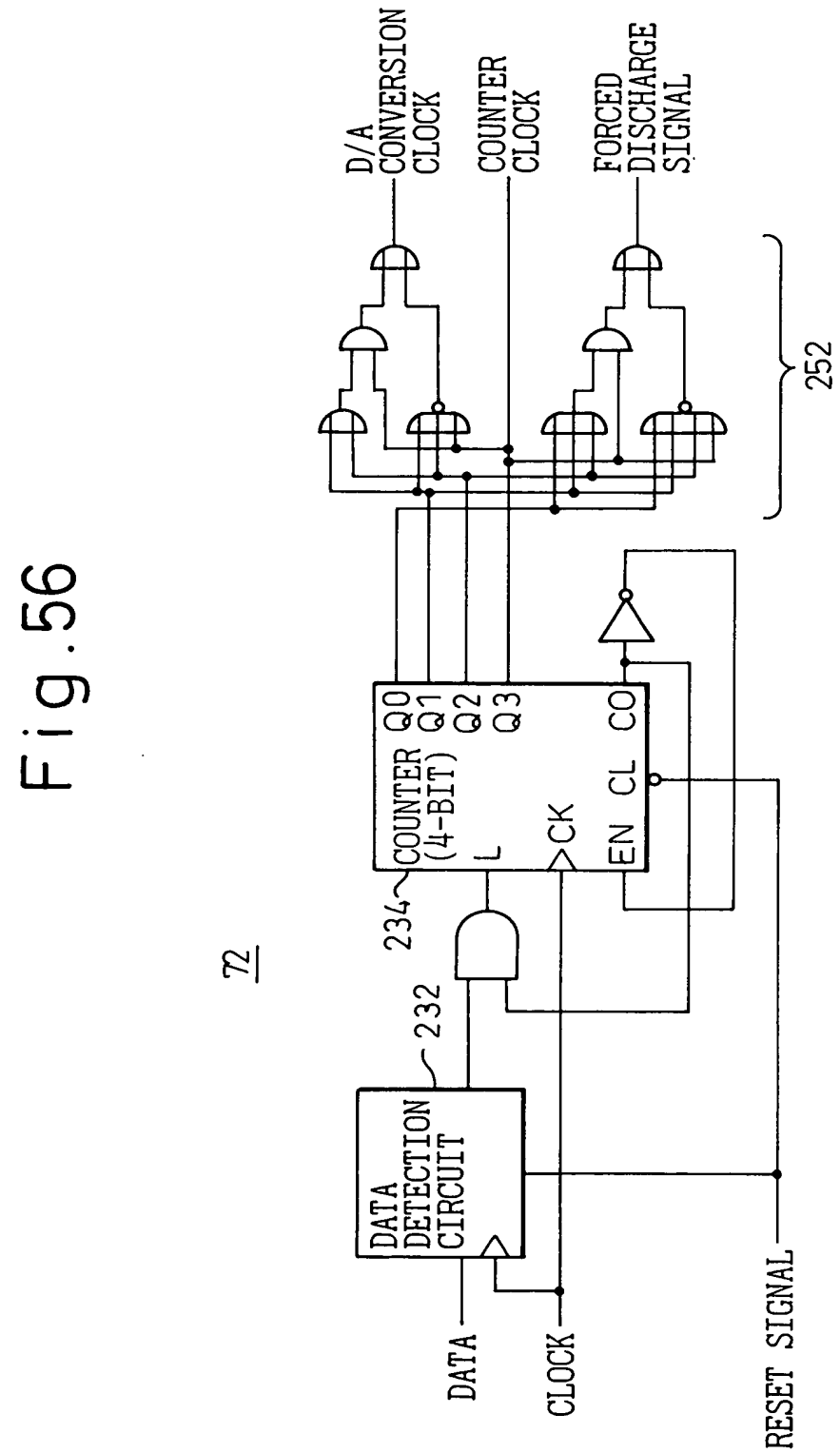

72
D/A CONVERSION CLOCK
COUNTER CLOCK
FORCED DISCHARGE SIGNAL
252
COUNTER (4-BIT)
Q0
Q1
Q2
Q3
L
CK
EN
CL
CO
234
232
DATA DETECTION CIRCUIT
DATA
CLOCK
RESET SIGNAL

Fig. 57

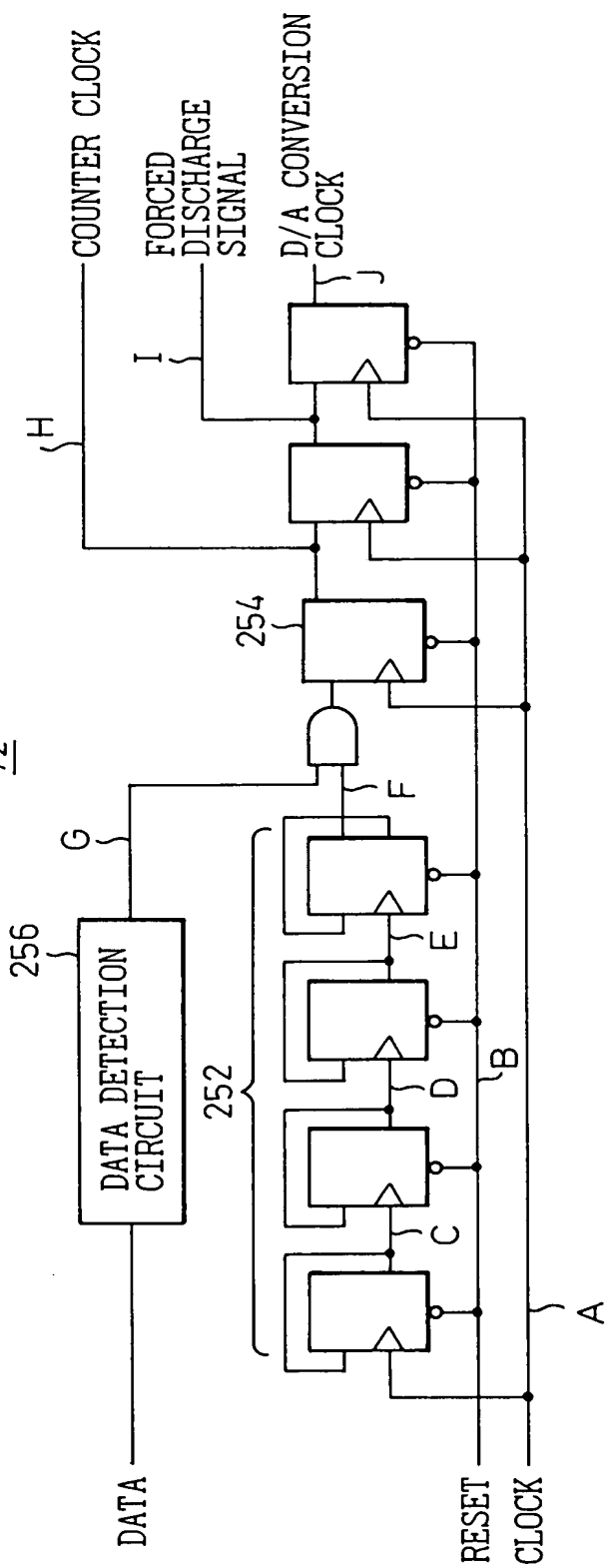

72
COUNTER CLOCK
FORCED DISCHARGE SIGNAL
D/A CONVERSION CLOCK
H
I
J
254
F
G
256
DATA DETECTION CIRCUIT
252
E
D
C
B
A
DATA
RESET
CLOCK

Fig.58

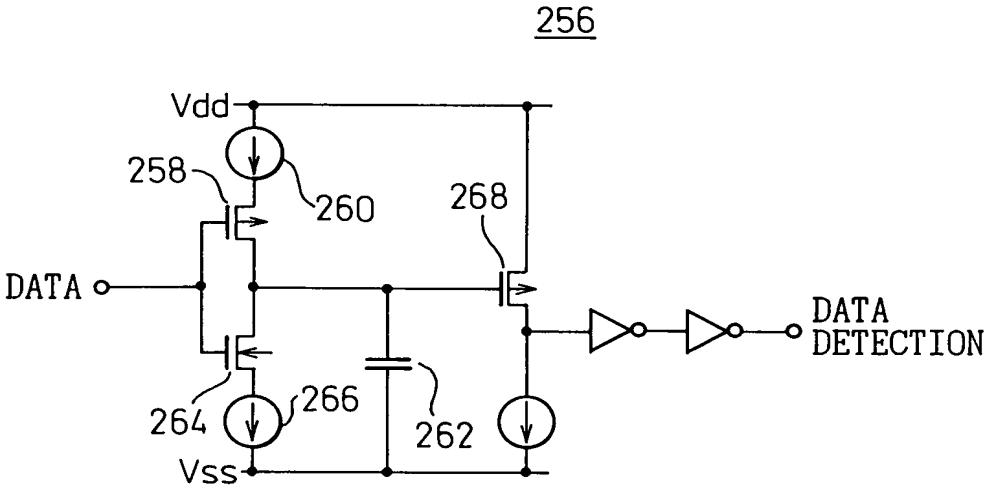


Fig.59

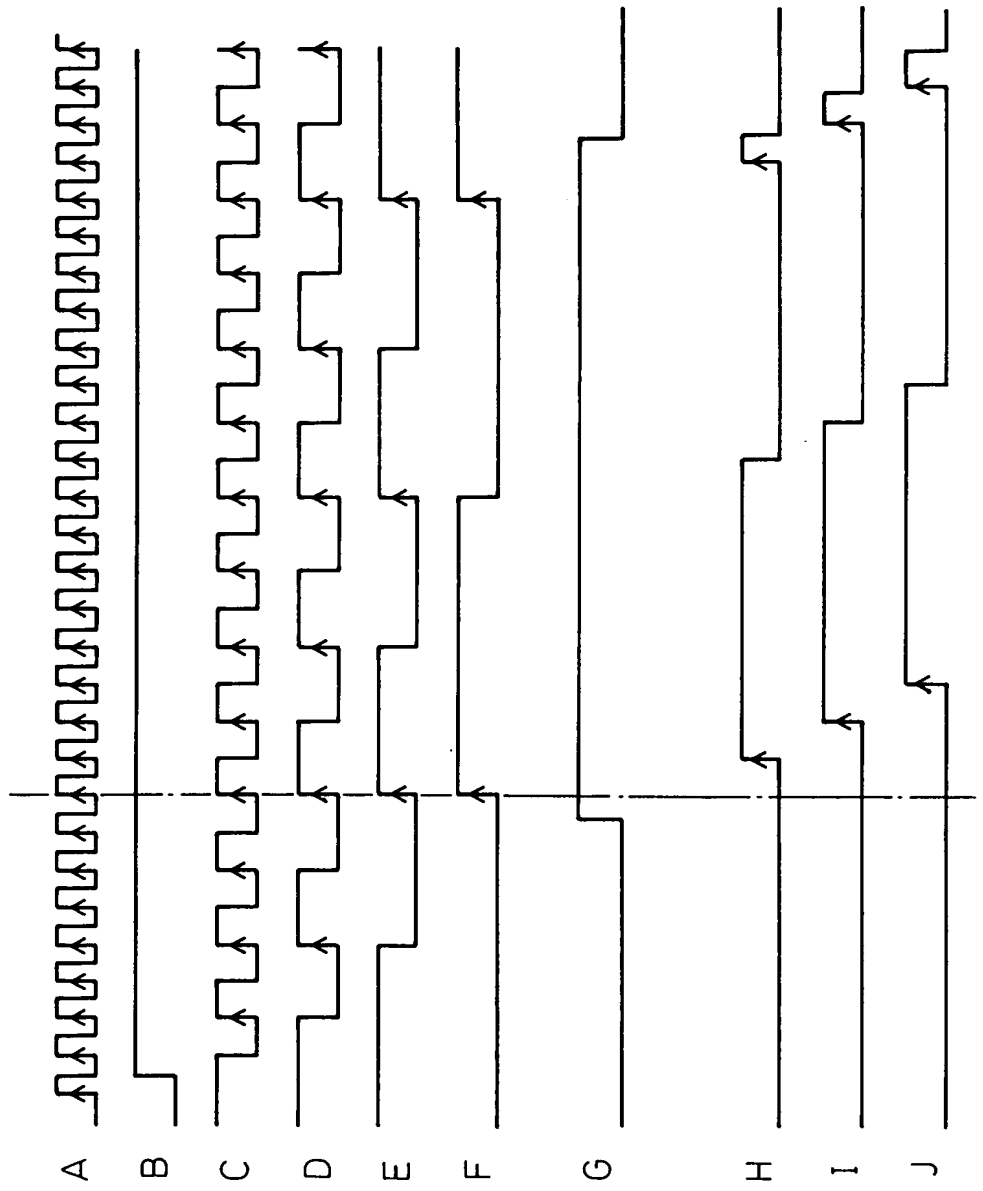


Fig.60

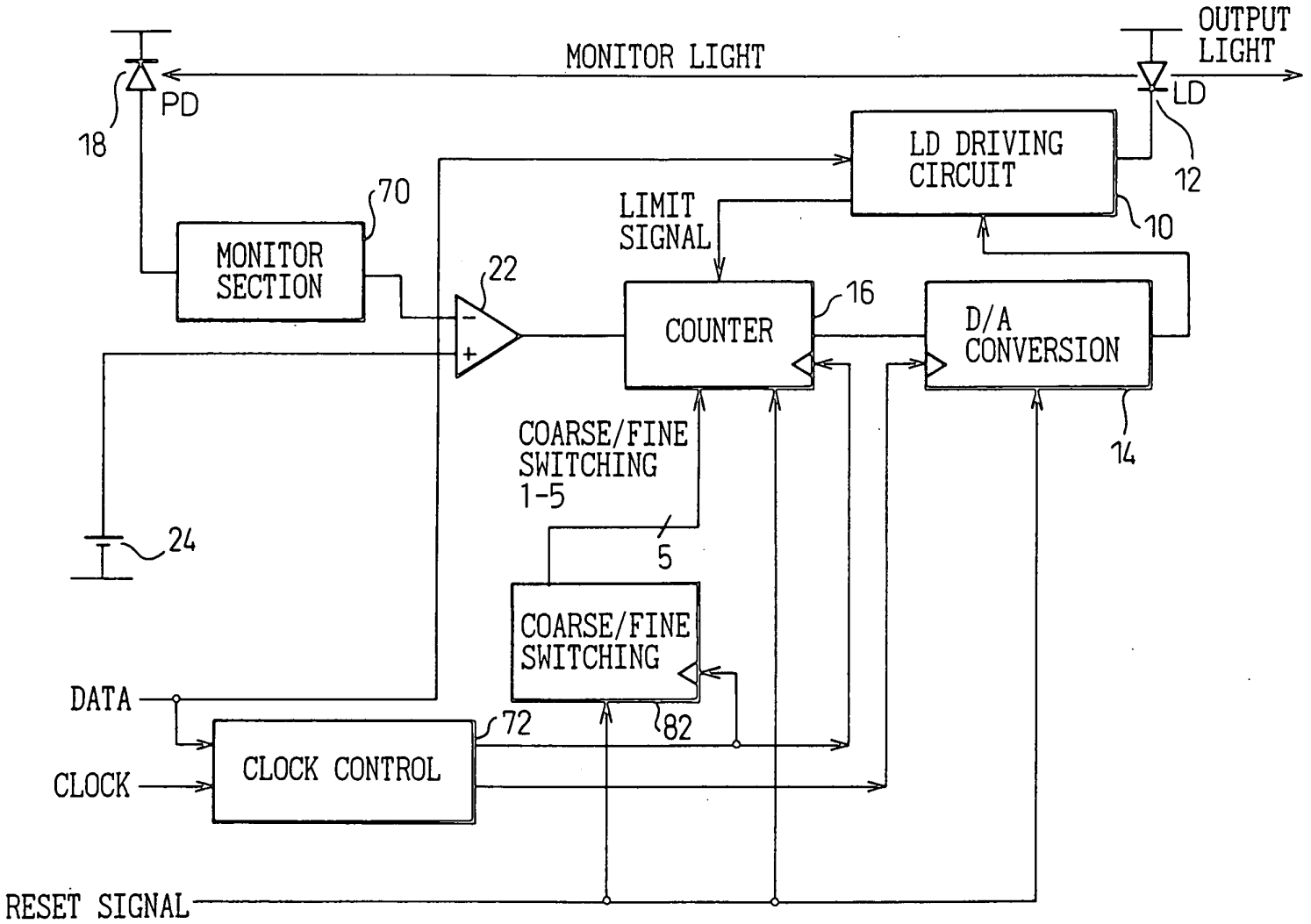

MONITOR LIGHT
OUTPUT LIGHT
PD
LD
18
12
LD DRIVING CIRCUIT
10
70
MONITOR SECTION
22
LIMIT SIGNAL
COUNTER
16
D/A CONVERSION
14
COARSE/FINE SWITCHING 1-5
5
24
COARSE/FINE SWITCHING
82
DATA
72
CLOCK
CLOCK CONTROL
RESET SIGNAL

Fig.61

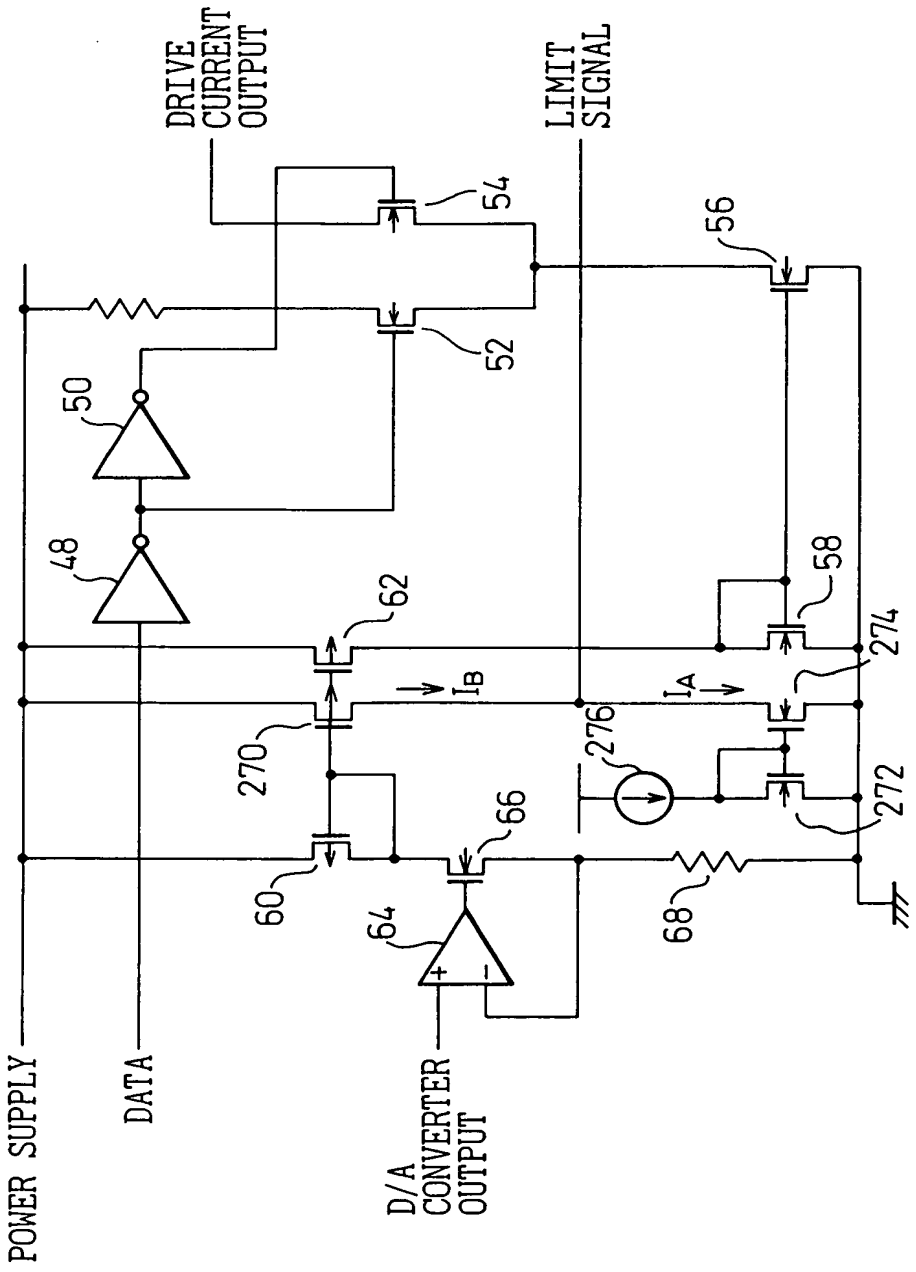

DRIVE CURRENT OUTPUT
LIMIT SIGNAL
POWER SUPPLY
DATA
D/A CONVERTER OUTPUT
48
50
52
54
56
58
60
62
64
66
68
270
272
274
276
$I_A$
$I_B$

Fig.62

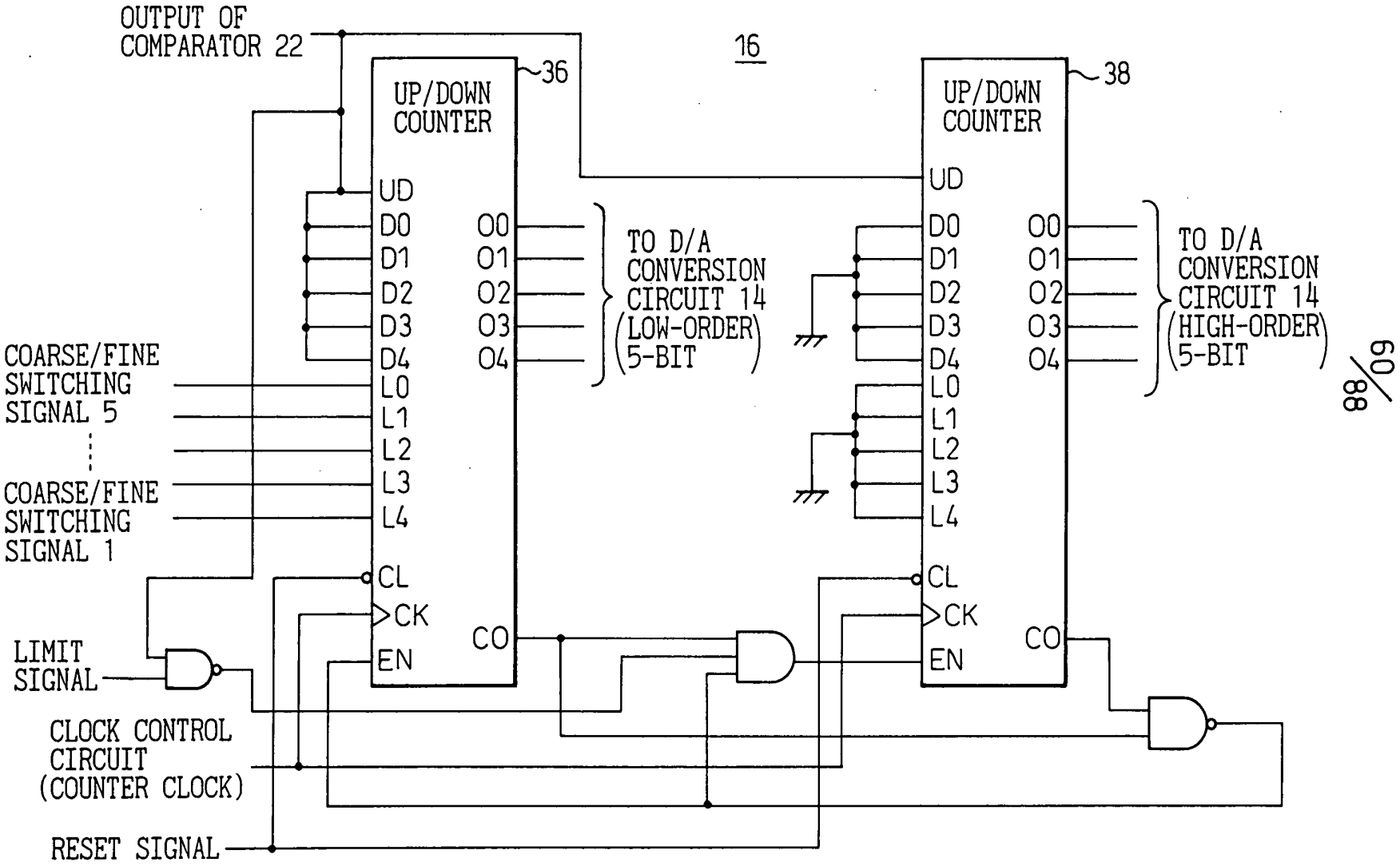

OUTPUT OF COMPARATOR 22
16
UP/DOWN COUNTER
36
UP/DOWN COUNTER
38
UD
D0
D1
D2
D3
D4
L0
L1
L2
L3
L4
CL
CK
EN
O0
O1
O2
O3
O4
CO
TO D/A CONVERSION CIRCUIT 14 (LOW-ORDER 5-BIT
TO D/A CONVERSION CIRCUIT 14 (HIGH-ORDER 5-BIT
COARSE/FINE SWITCHING SIGNAL 5
COARSE/FINE SWITCHING SIGNAL 1
LIMIT SIGNAL
CLOCK CONTROL CIRCUIT (COUNTER CLOCK)
RESET SIGNAL

Fig.63

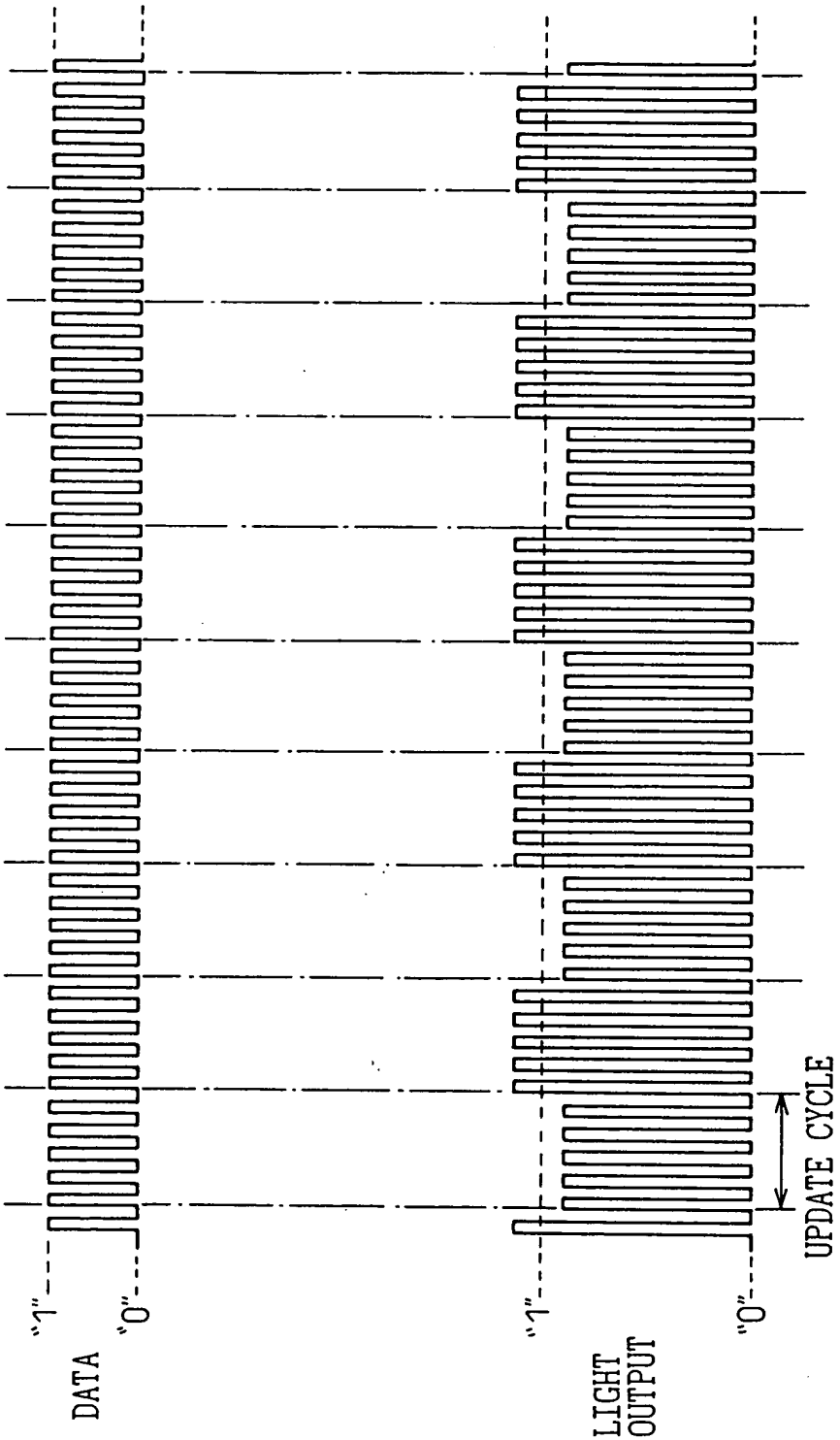


Fig.64

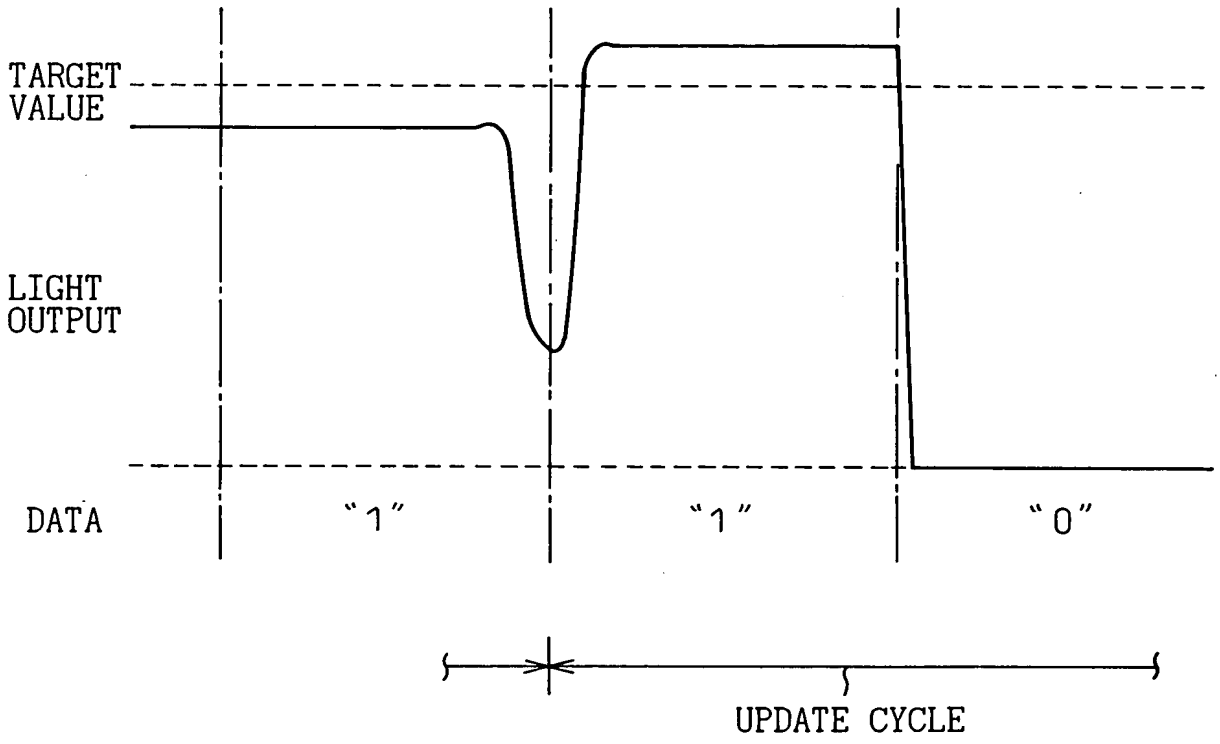


Fig.65

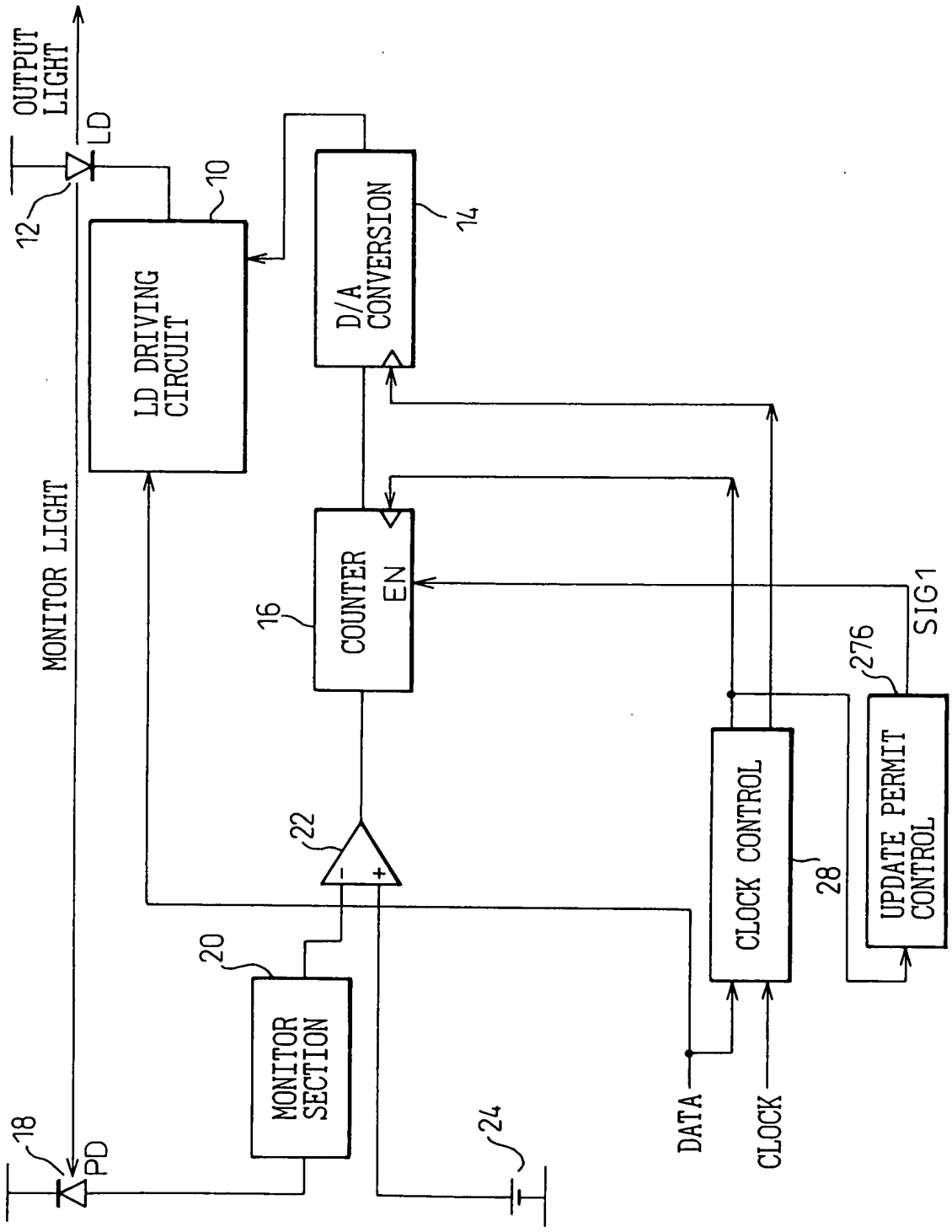

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
D/A CONVERSION
14
MONITOR LIGHT
16
COUNTER
EN
SIG1
276
22
-
+
20
MONITOR SECTION
CLOCK CONTROL
28
UPDATE PERMIT CONTROL
18
PD
24
DATA
CLOCK

Fig.66

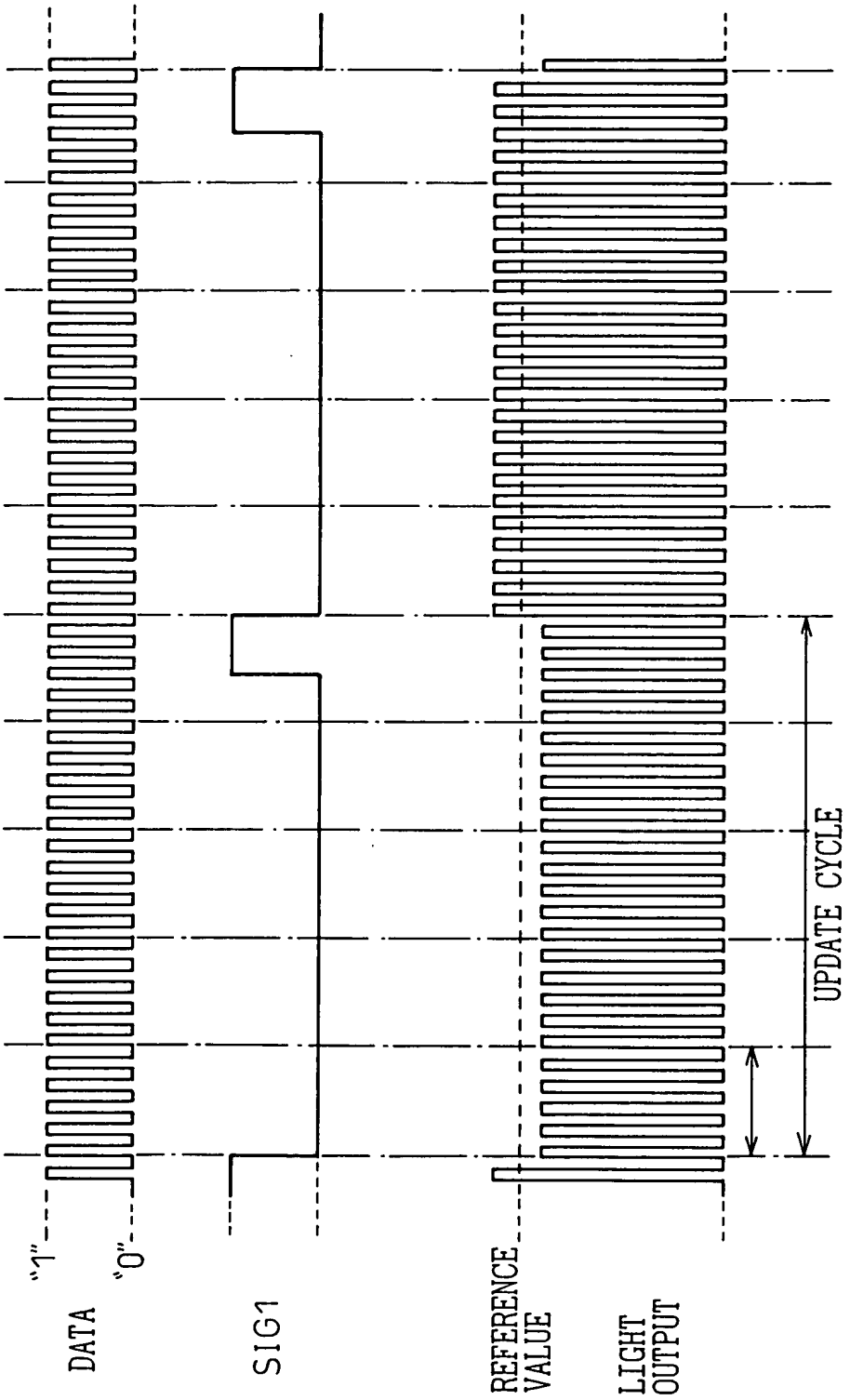


Fig.67

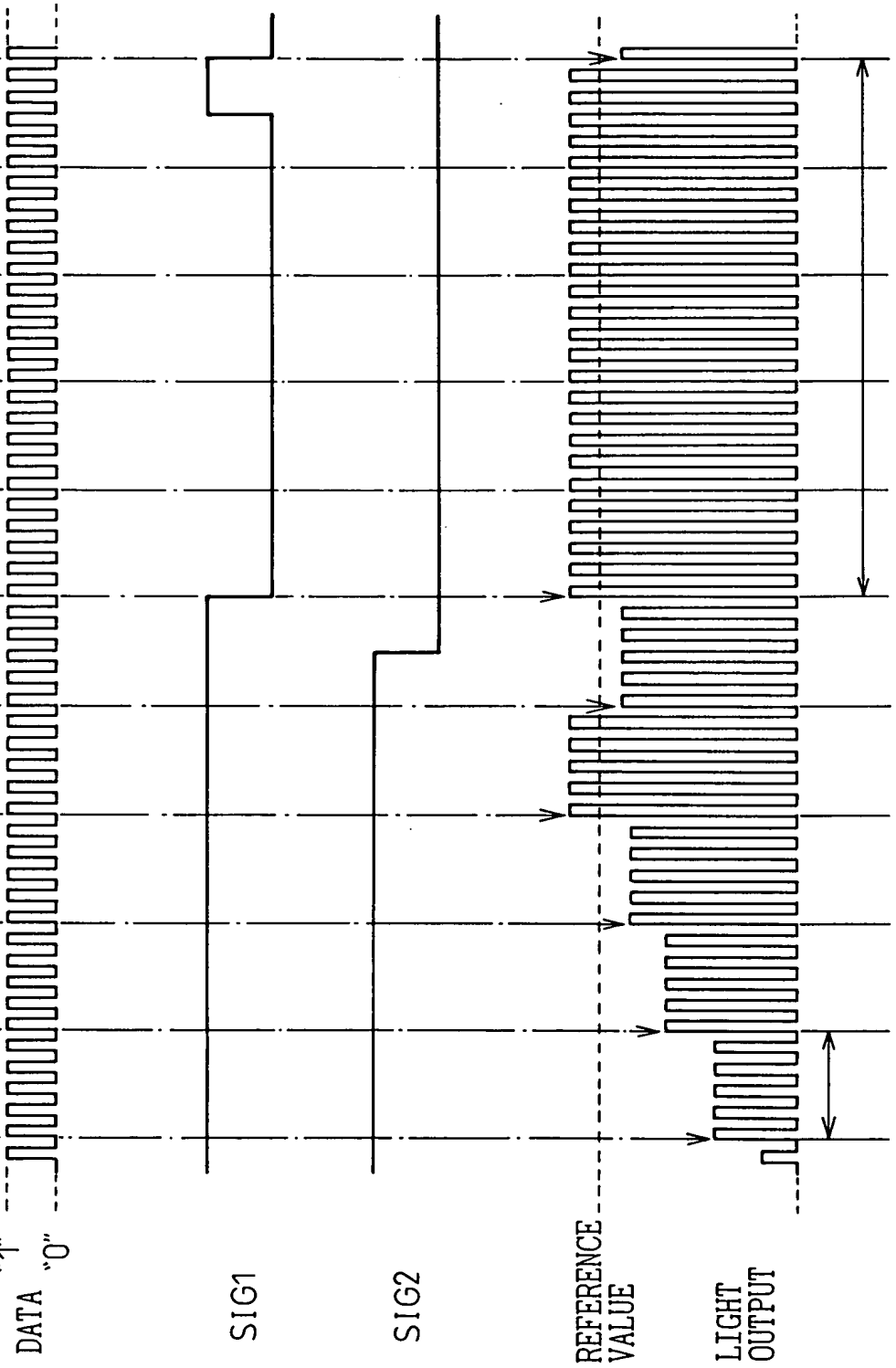


Fig.68

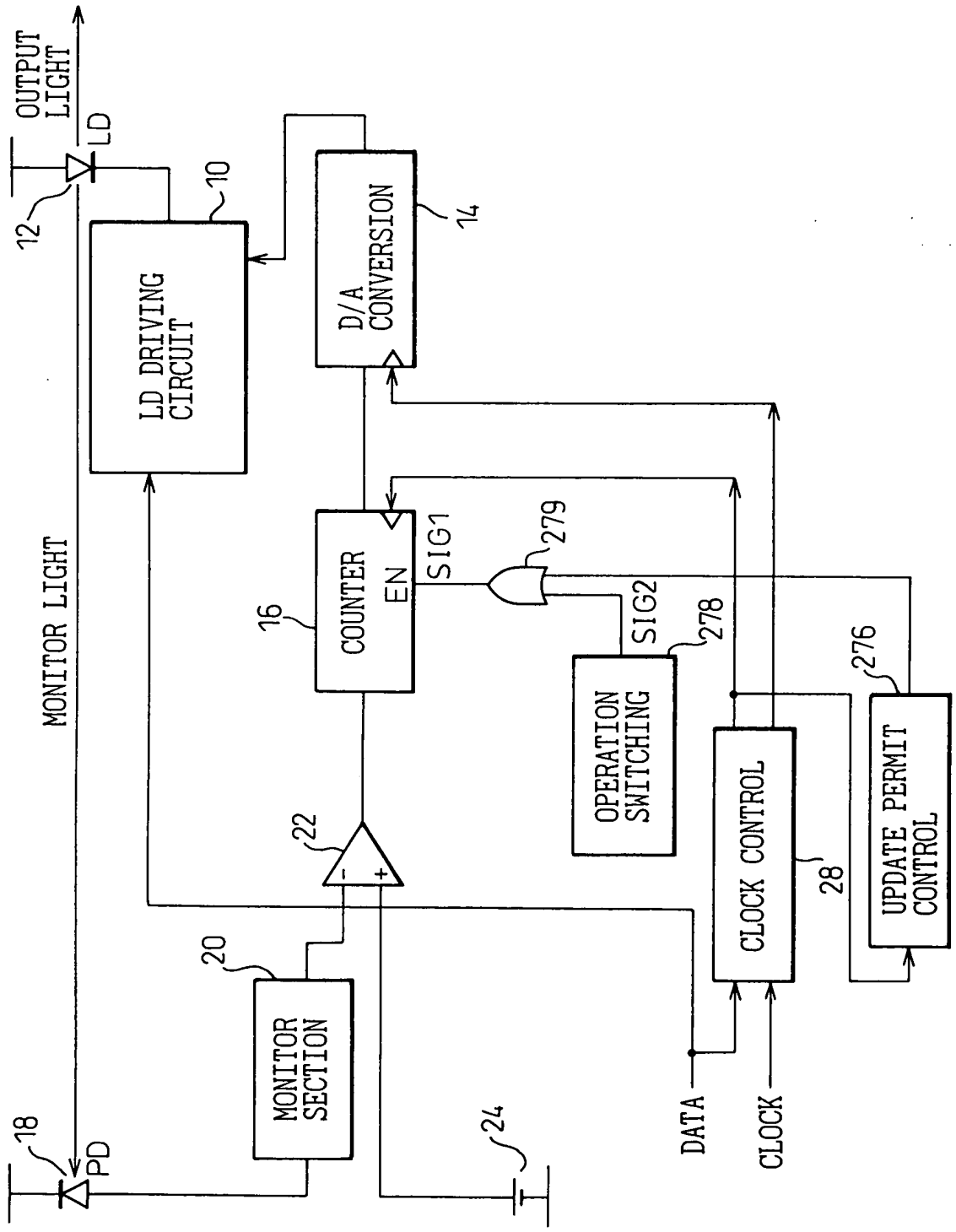

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
D/A CONVERSION
14
MONITOR LIGHT
16
COUNTER
EN
SIG1
279
SIG2
278
OPERATION SWITCHING
276
CLOCK CONTROL
28
UPDATE PERMIT CONTROL
22
-
+
20
MONITOR SECTION
18
PD
24
DATA
CLOCK

Fig.69

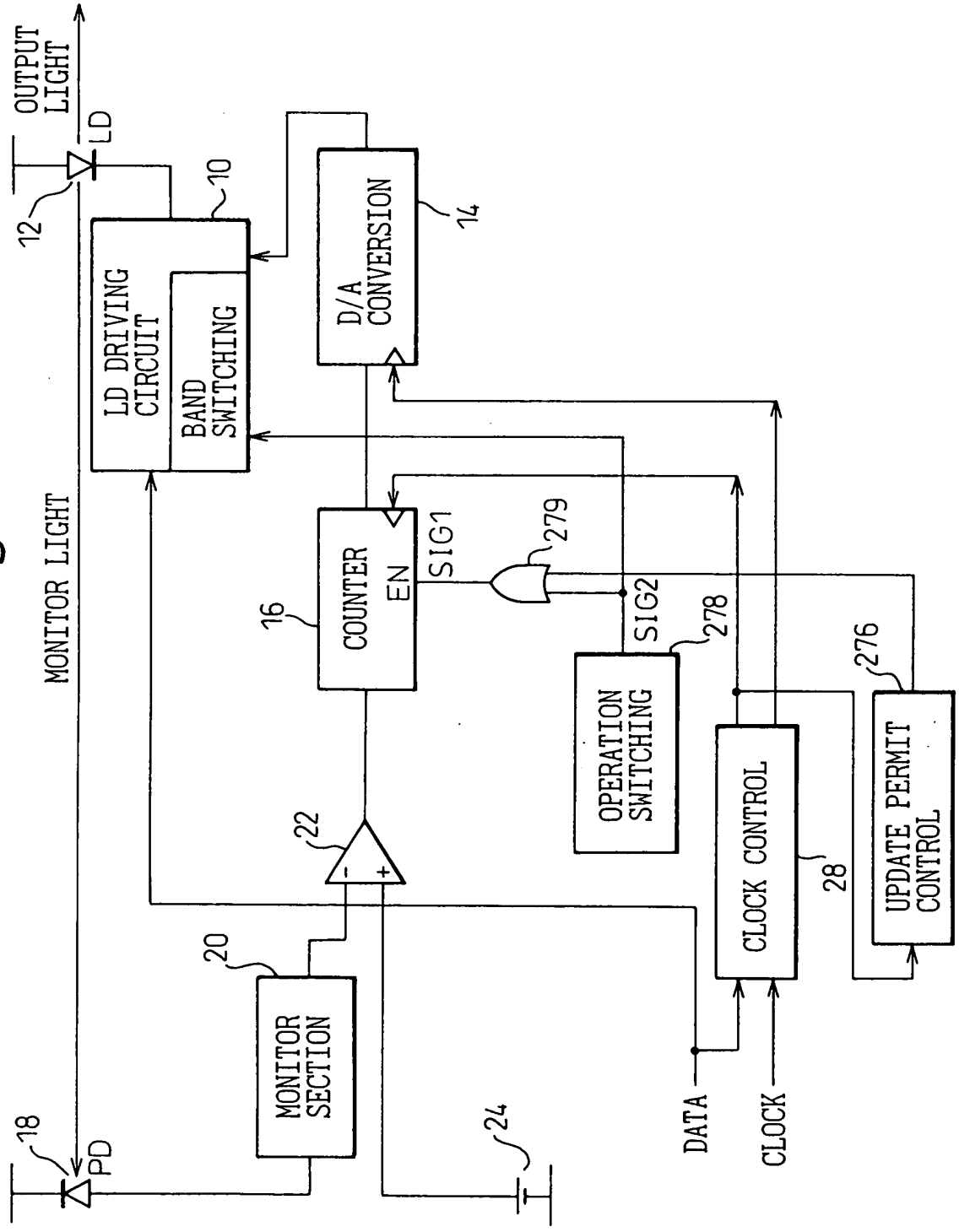

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
BAND SWITCHING
D/A CONVERSION
14
MONITOR LIGHT
16
COUNTER
EN
SIG1
279
SIG2
278
OPERATION SWITCHING
276
UPDATE PERMIT CONTROL
CLOCK CONTROL
28
22
20
MONITOR SECTION
18
PD
24
DATA
CLOCK

Fig.70

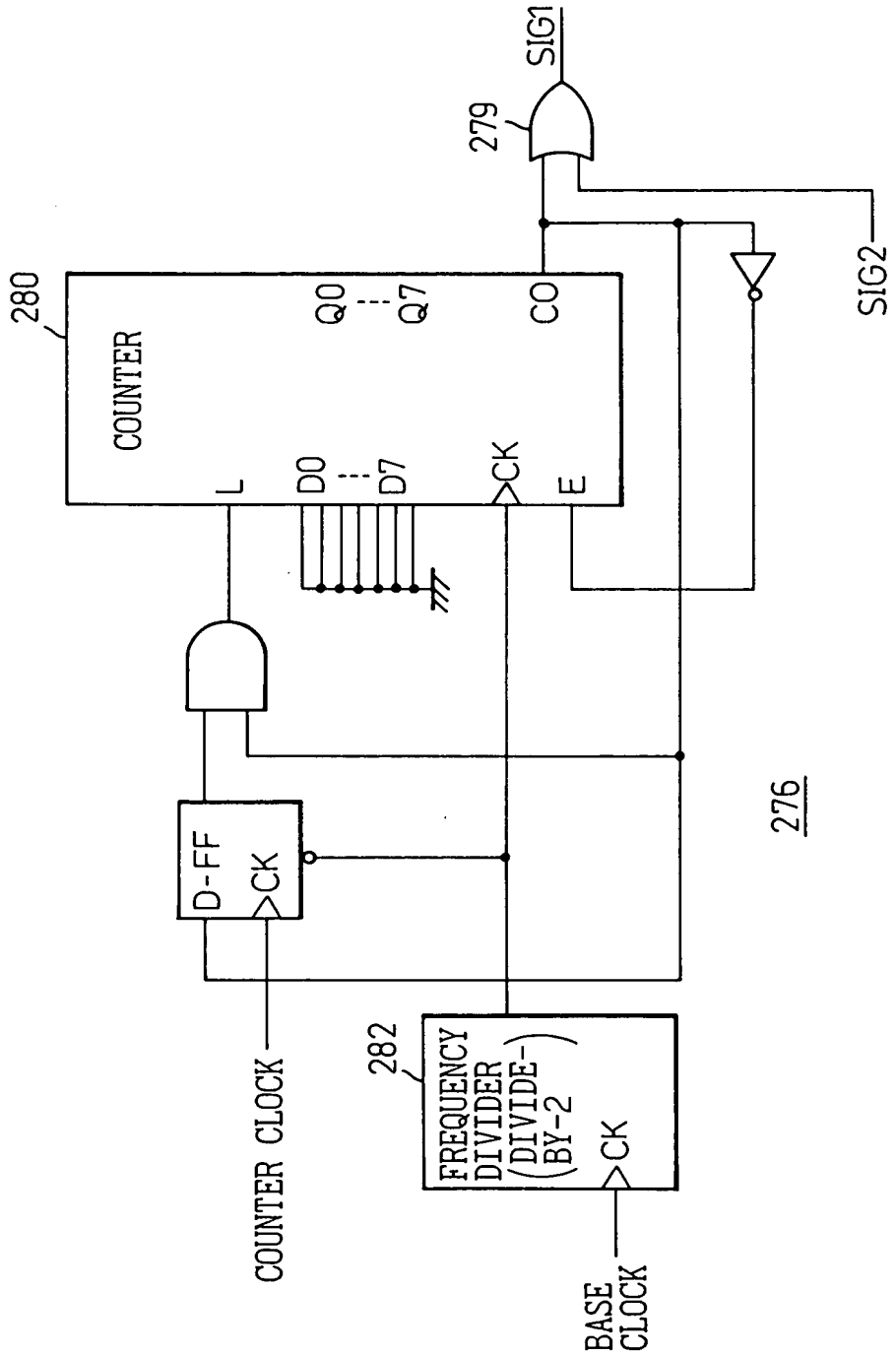

SIG1
279
SIG2
280
COUNTER
Q0
Q7
CO
L
D0
D7
CK
E
D-FF
CK
COUNTER CLOCK
282
FREQUENCY DIVIDER (DIVIDE-BY-2)
CK
BASE CLOCK
276

Fig.71

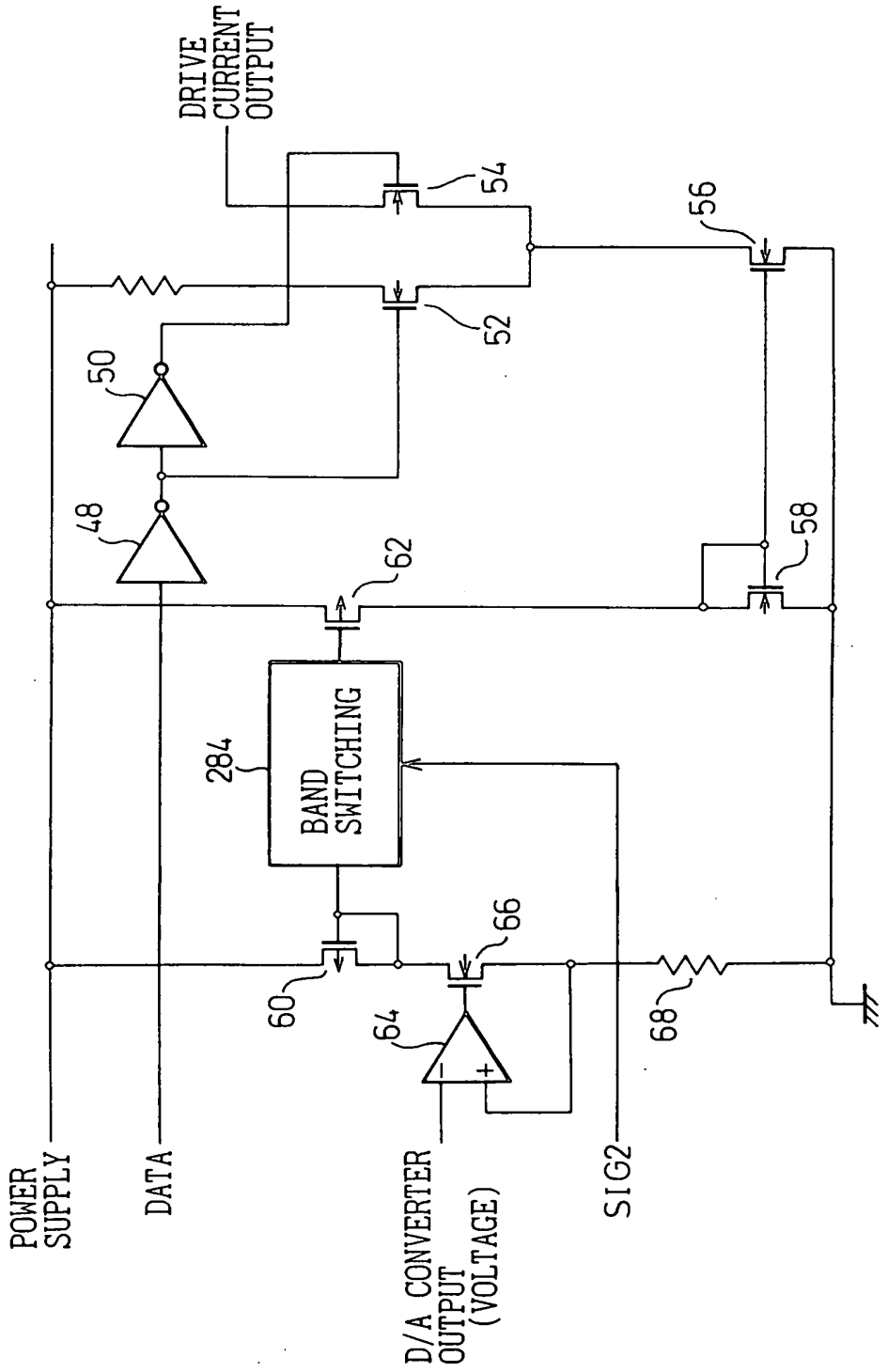

DRIVE CURRENT OUTPUT
54
56
52
50
48
62
58
284
BAND SWITCHING
66
60
64
68
POWER SUPPLY
DATA
D/A CONVERTER OUTPUT (VOLTAGE)
SIG2

Fig.72

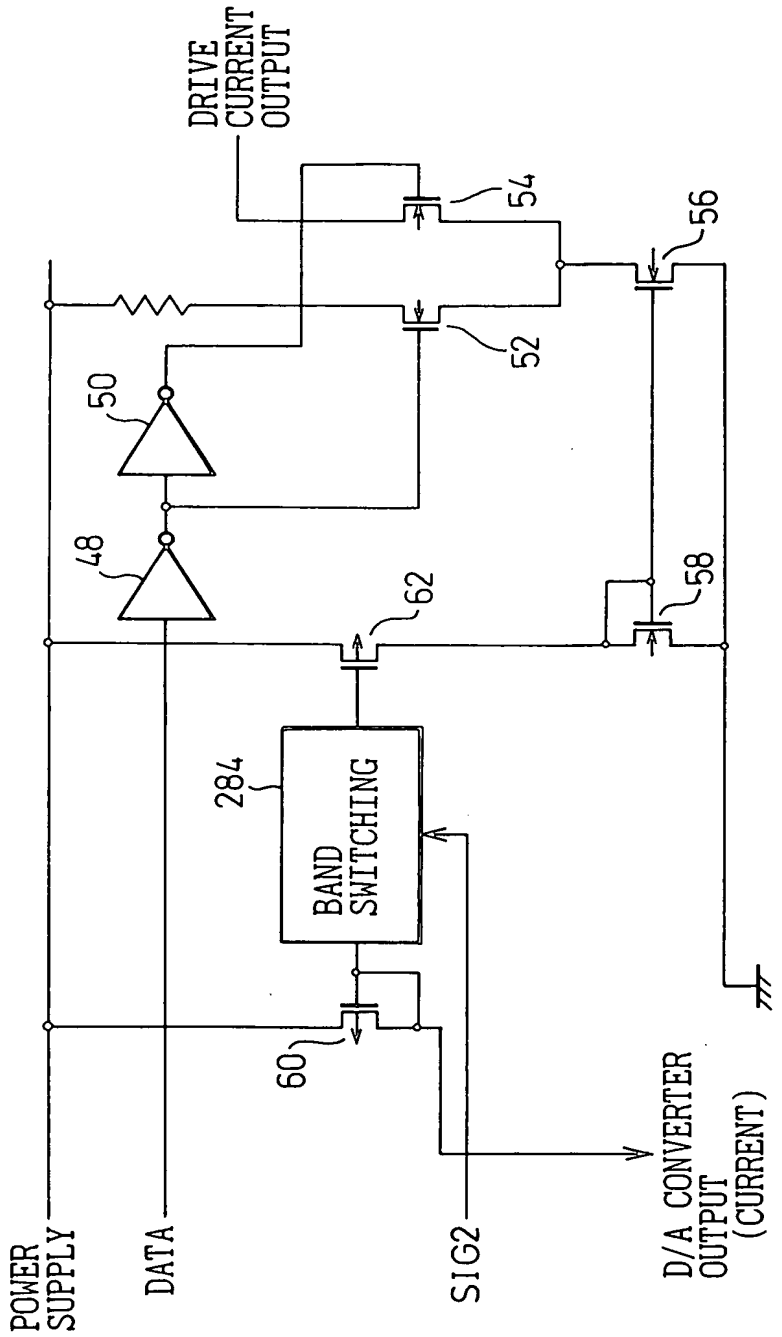

DRIVE CURRENT OUTPUT
54
56
52
50
48
62
58
284
BAND SWITCHING
60
POWER SUPPLY
DATA
SIG2
D/A CONVERTER OUTPUT (CURRENT)

Fig. 73

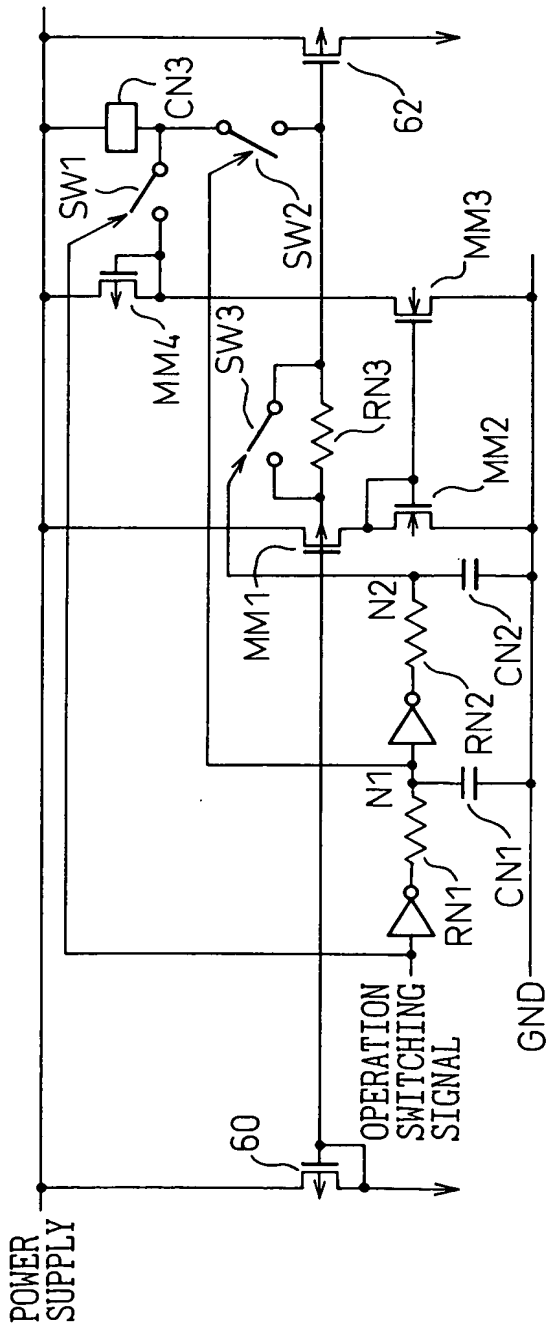

POWER SUPPLY
60
OPERATION SWITCHING SIGNAL
GND
62
CN3
SW1
SW2
SW3
MM4
MM3
MM2
MM1
RN3
N2
CN2
RN2
N1
RN1
CN1

Fig. 74

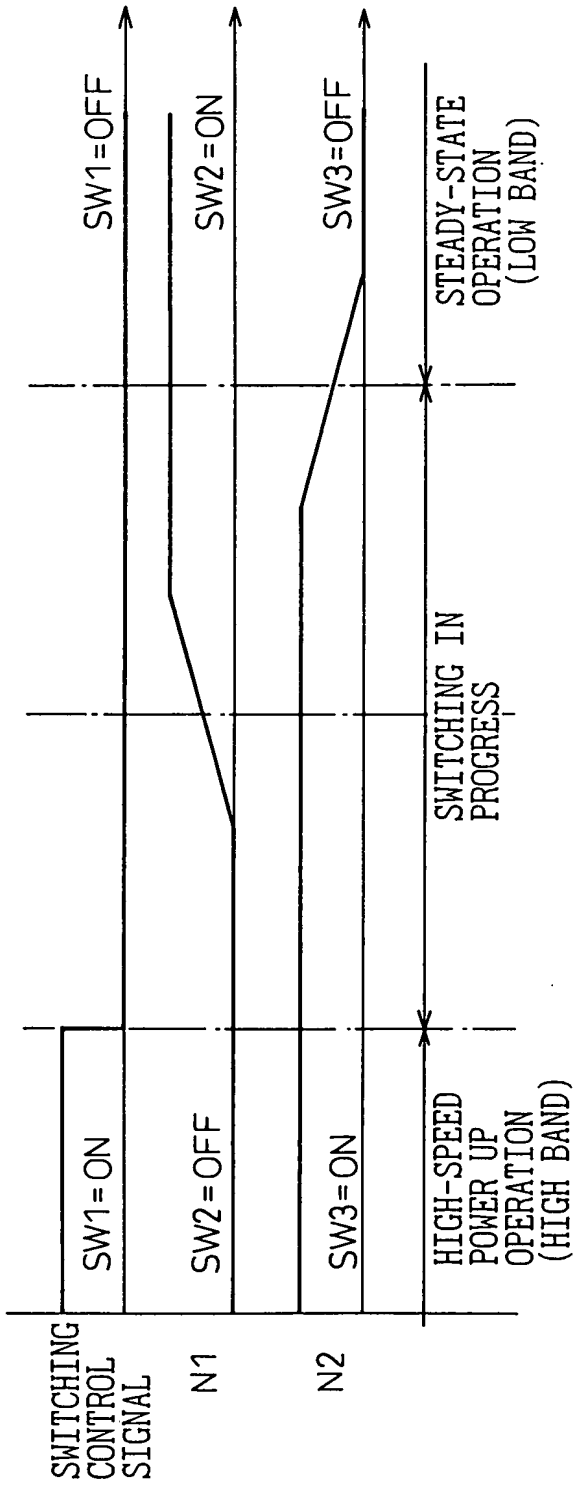

SWITCHING CONTROL SIGNAL
SW1=ON
SW2=OFF
SW3=ON
N1
N2
SW1=OFF
SW2=ON
SW3=OFF
HIGH-SPEED POWER UP OPERATION (HIGH BAND)
SWITCHING IN PROGRESS
STEADY-STATE OPERATION (LOW BAND)

Fig.75

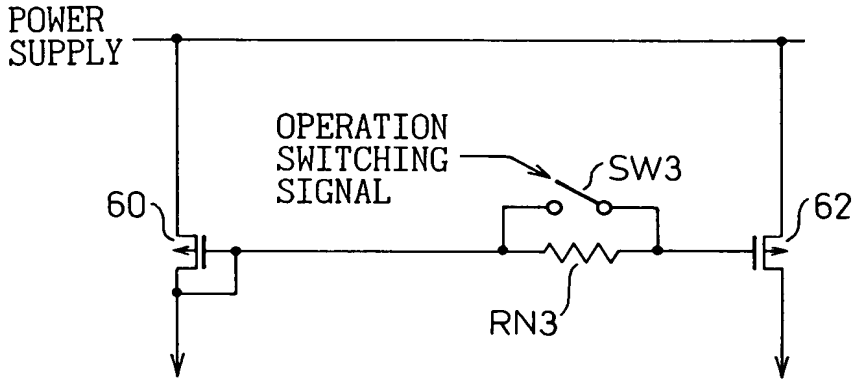

POWER
SUPPLY
OPERATION
SWITCHING
SIGNAL
SW3
60
62
RN3

Fig.76

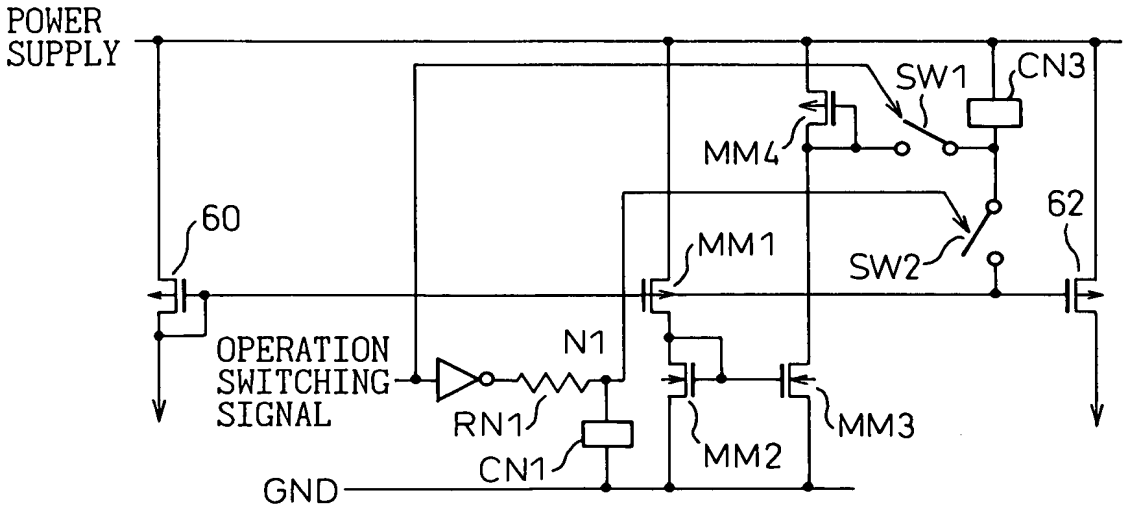

POWER
SUPPLY
SW1
CN3
MM4
60
62
MM1
SW2
OPERATION
SWITCHING
SIGNAL
N1
RN1
CN1
MM2
MM3
GND

Fig.77

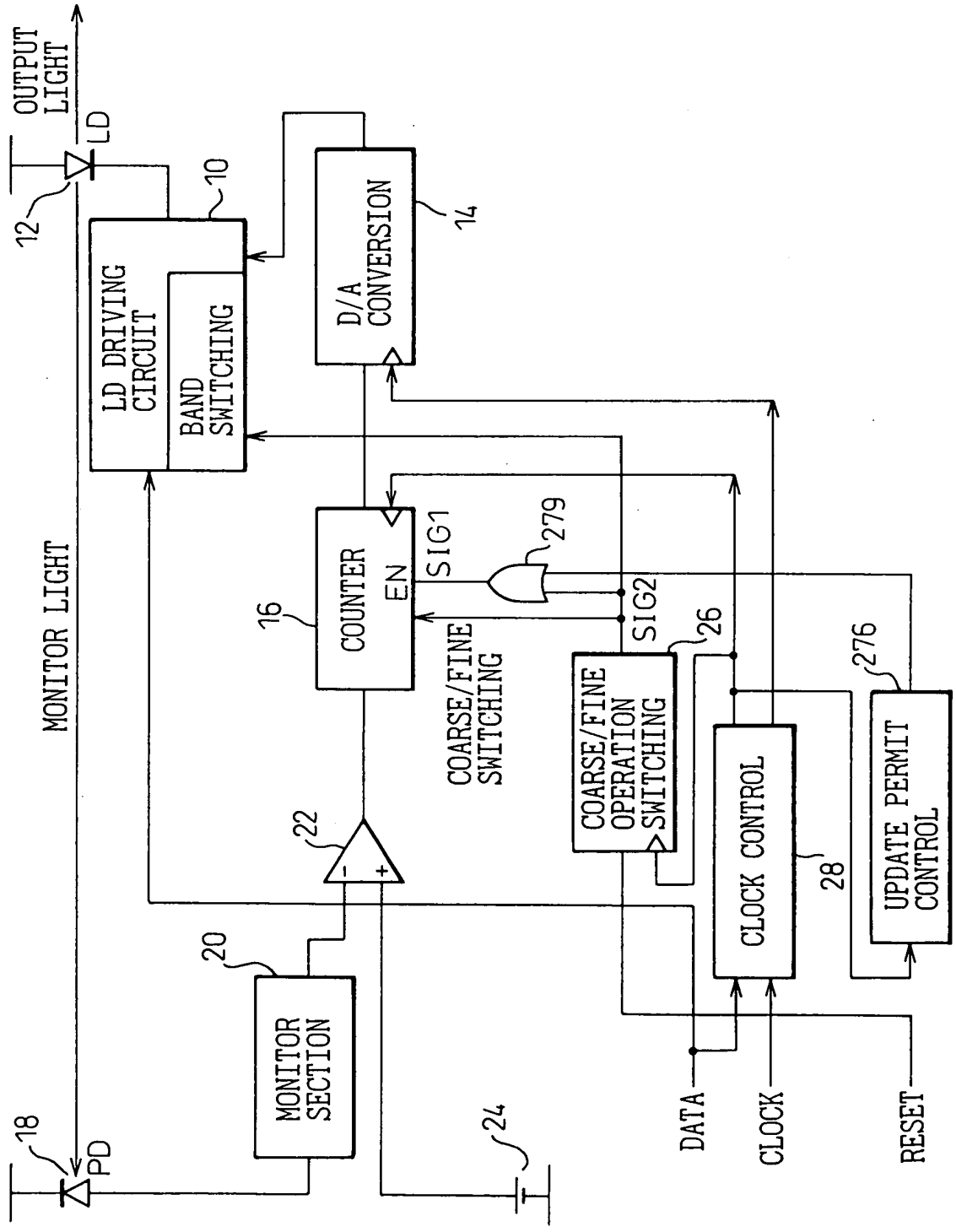

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
BAND SWITCHING
D/A CONVERSION
14
MONITOR LIGHT
16
COUNTER
EN
SIG1
279
SIG2
26
COARSE/FINE SWITCHING
COARSE/FINE OPERATION SWITCHING
276
CLOCK CONTROL
28
UPDATE PERMIT CONTROL
22
20
MONITOR SECTION
18
PD
24
DATA
CLOCK
RESET

Fig.78

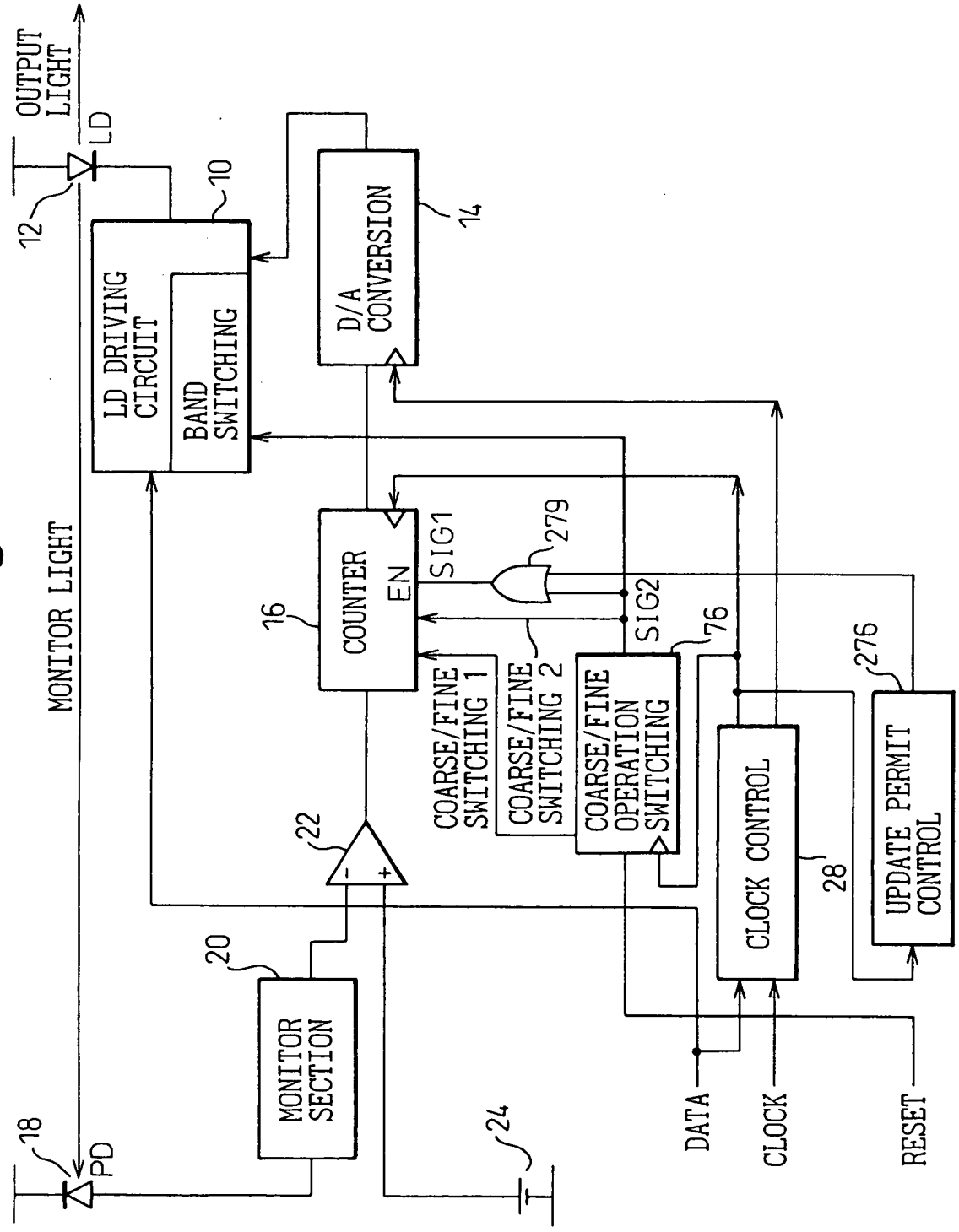

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
BAND SWITCHING
D/A CONVERSION
14
MONITOR LIGHT
16
COUNTER
EN
SIG1
279
SIG2
76
276
COARSE/FINE SWITCHING 1
COARSE/FINE SWITCHING 2
COARSE/FINE OPERATION SWITCHING
CLOCK CONTROL
28
UPDATE PERMIT CONTROL
22
20
MONITOR SECTION
18
PD
24
DATA
CLOCK
RESET

Fig.79

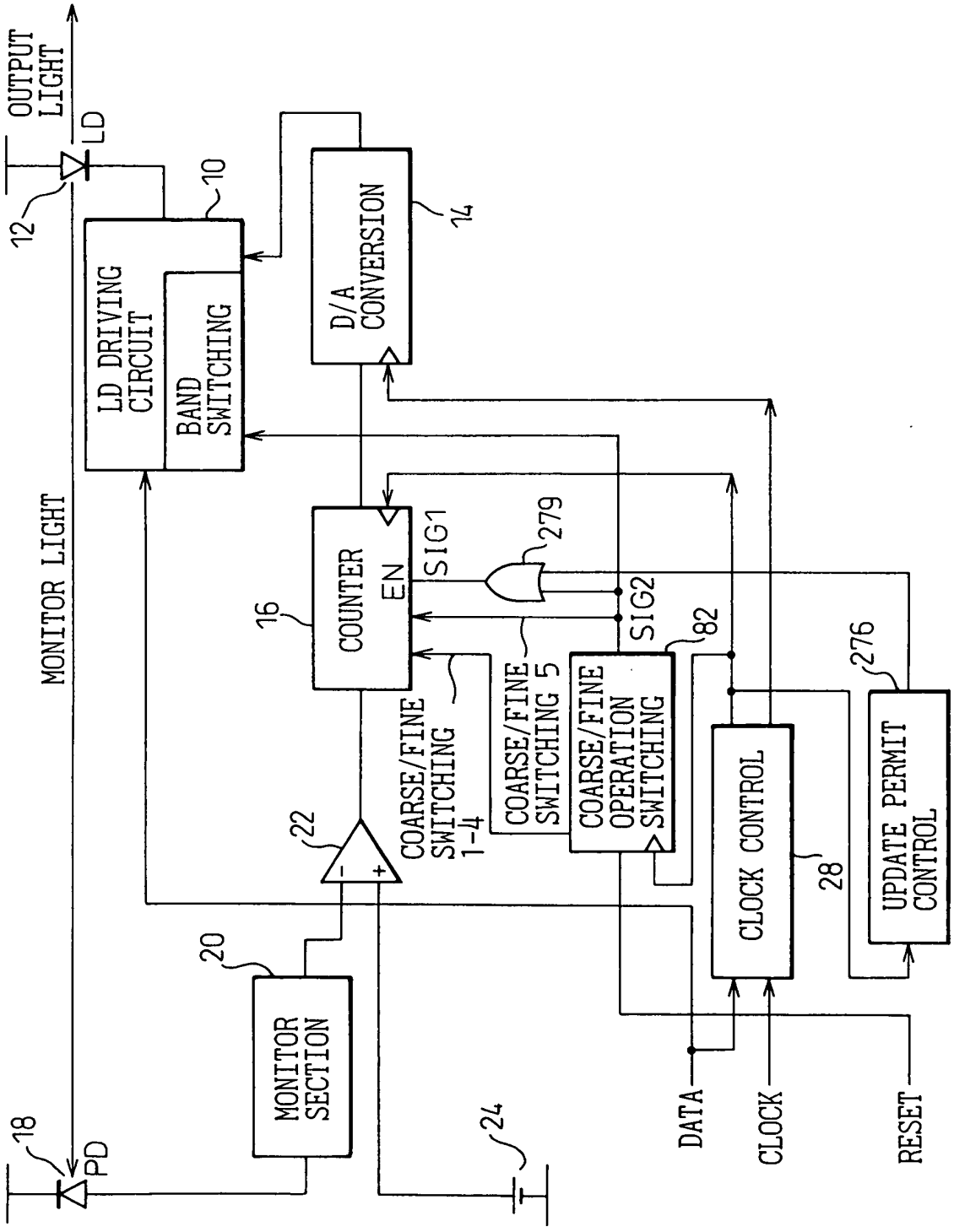

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
BAND SWITCHING
D/A CONVERSION
14
MONITOR LIGHT
16
COUNTER
EN
SIG1
279
SIG2
82
276
COARSE/FINE SWITCHING 1-4
COARSE/FINE SWITCHING 5
COARSE/FINE OPERATION SWITCHING
22
CLOCK CONTROL
28
UPDATE PERMIT CONTROL
20
MONITOR SECTION
18
PD
24
DATA
CLOCK
RESET

Fig.80

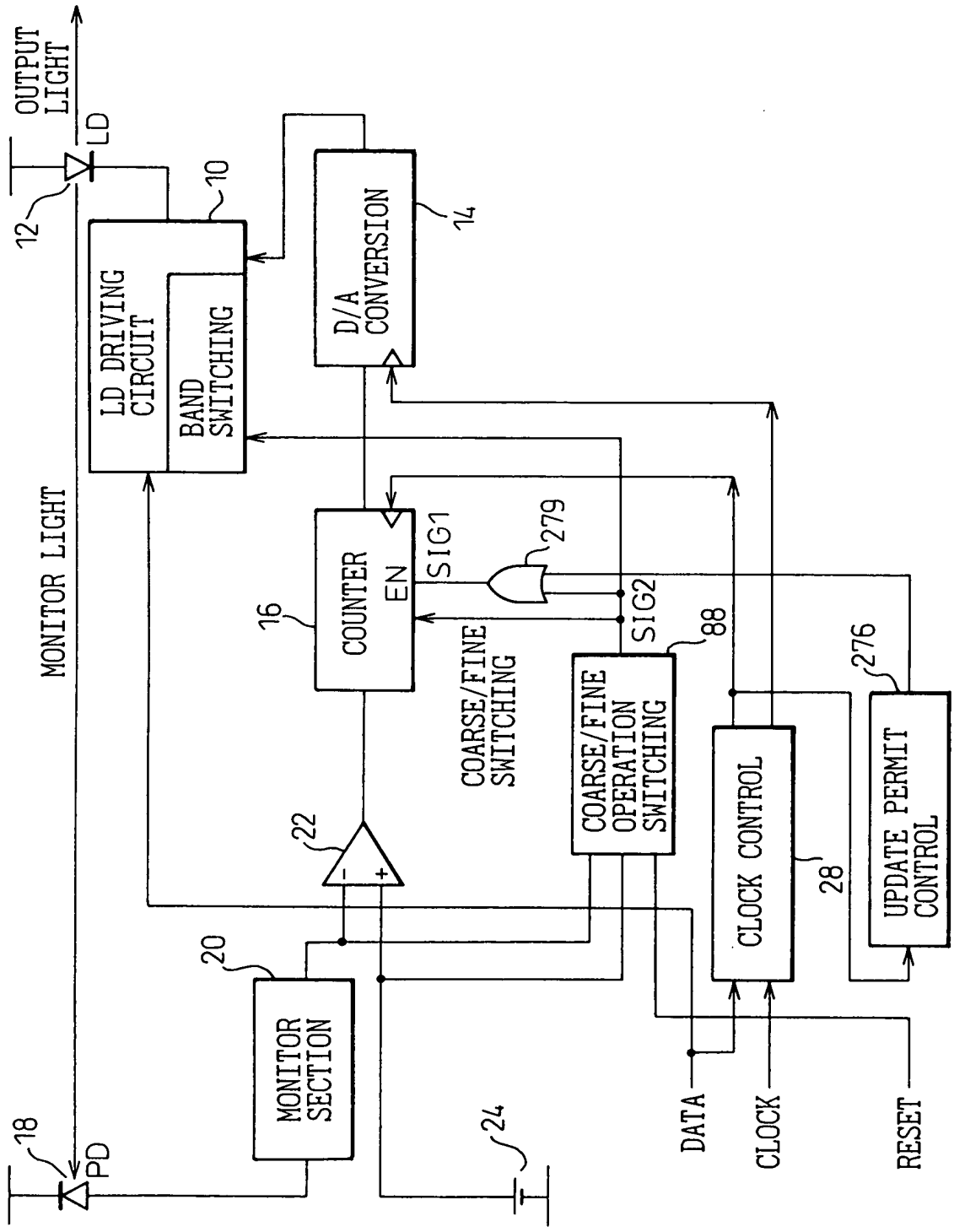

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
BAND SWITCHING
D/A CONVERSION
14
MONITOR LIGHT
16
COUNTER
EN
SIG1
279
SIG2
88
COARSE/FINE SWITCHING
COARSE/FINE OPERATION SWITCHING
276
UPDATE PERMIT CONTROL
CLOCK CONTROL
28
22
20
MONITOR SECTION
18
PD
24
DATA
CLOCK
RESET

Fig. 81

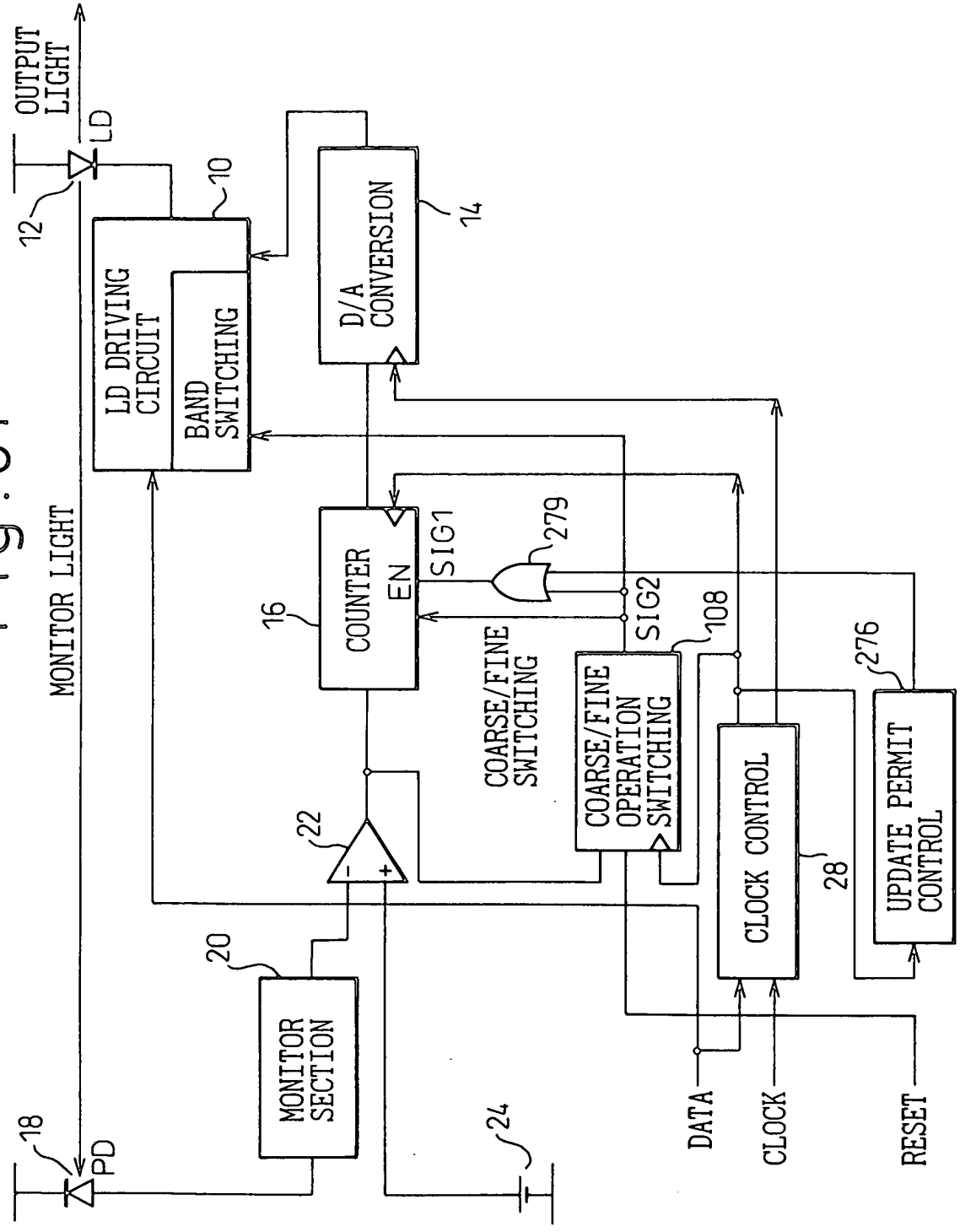

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
BAND SWITCHING
D/A CONVERSION
14
MONITOR LIGHT
16
COUNTER
EN
SIG1
279
SIG2
108
276
COARSE/FINE SWITCHING
COARSE/FINE OPERATION SWITCHING
22
CLOCK CONTROL
28
UPDATE PERMIT CONTROL
20
MONITOR SECTION
18
PD
24
DATA
CLOCK
RESET

Fig.82

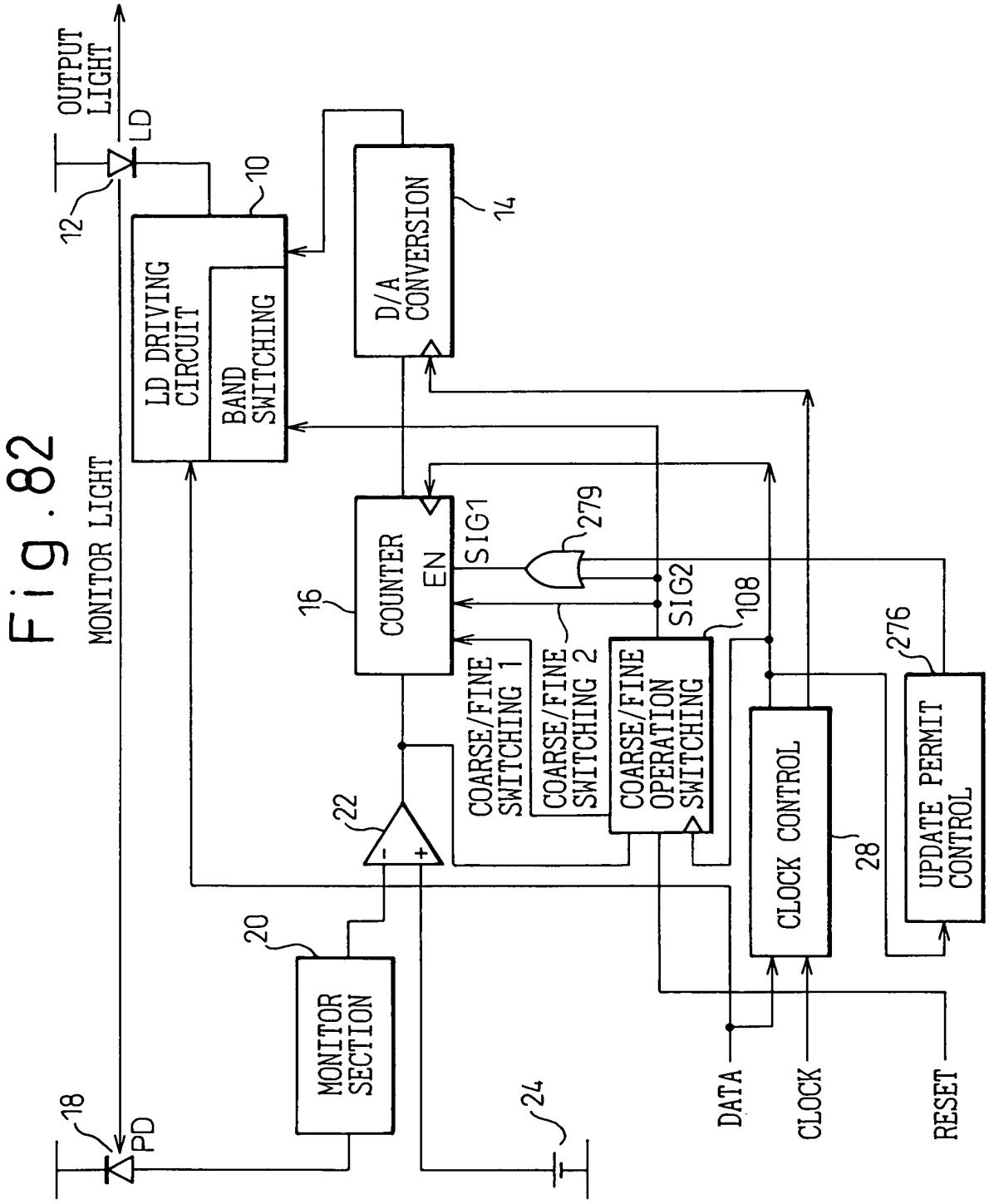

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
BAND SWITCHING
D/A CONVERSION
14
MONITOR LIGHT
16
COUNTER
EN
SIG1
279
SIG2
108
276
COARSE/FINE SWITCHING 1
COARSE/FINE SWITCHING 2
COARSE/FINE OPERATION SWITCHING
CLOCK CONTROL
28
UPDATE PERMIT CONTROL
22
20
MONITOR SECTION
18
PD
24
DATA
CLOCK
RESET

Fig.83

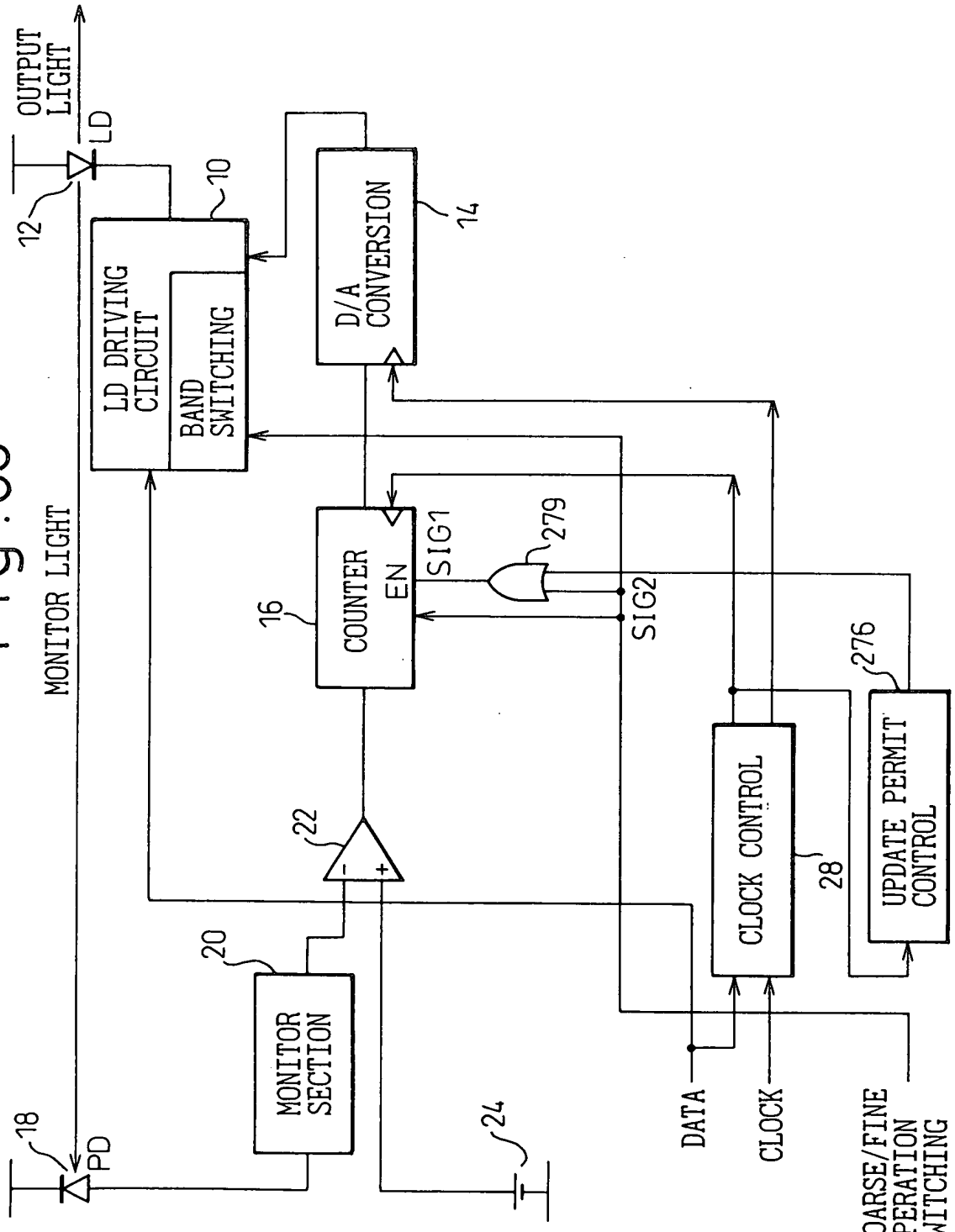

OUTPUT LIGHT
LD
12
10
LD DRIVING CIRCUIT
BAND SWITCHING
D/A CONVERSION
14
MONITOR LIGHT
16
COUNTER
EN
SIG1
279
SIG2
276
22
20
MONITOR SECTION
CLOCK CONTROL
28
UPDATE PERMIT CONTROL
18
PD
24
DATA
CLOCK
COARSE/FINE OPERATION SWITCHING

Fig.84

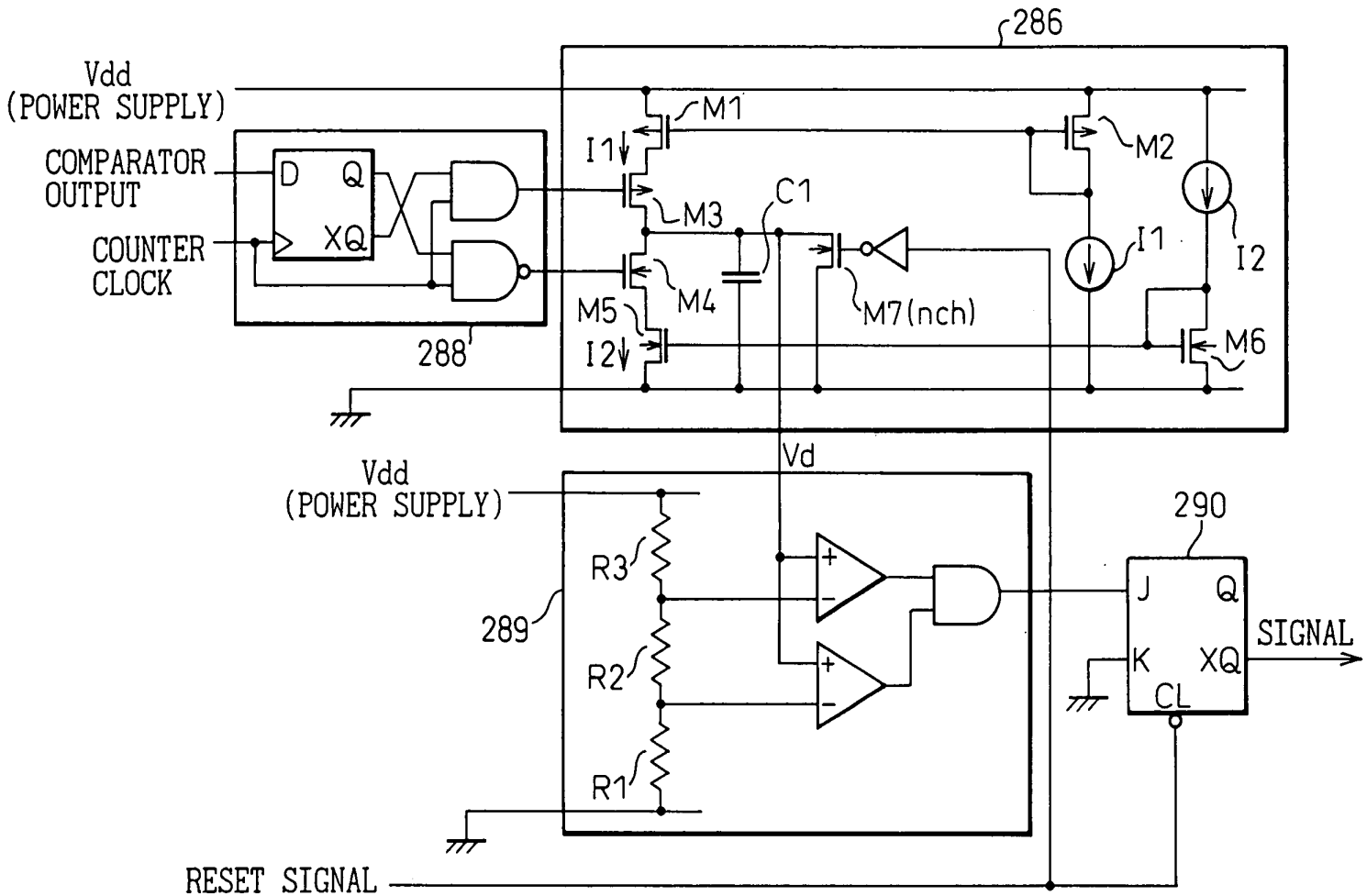

286
Vdd
(POWER SUPPLY)
COMPARATOR
OUTPUT
COUNTER
CLOCK
D
Q
XQ
288
M1
I1
M2
M3
C1
I1
I2
M4
M5
I2
M7(nch)
M6
Vd
Vdd
(POWER SUPPLY)
290
R3
289
R2
R1
J
Q
K
XQ
CL
SIGNAL
RESET SIGNAL

Fig.85

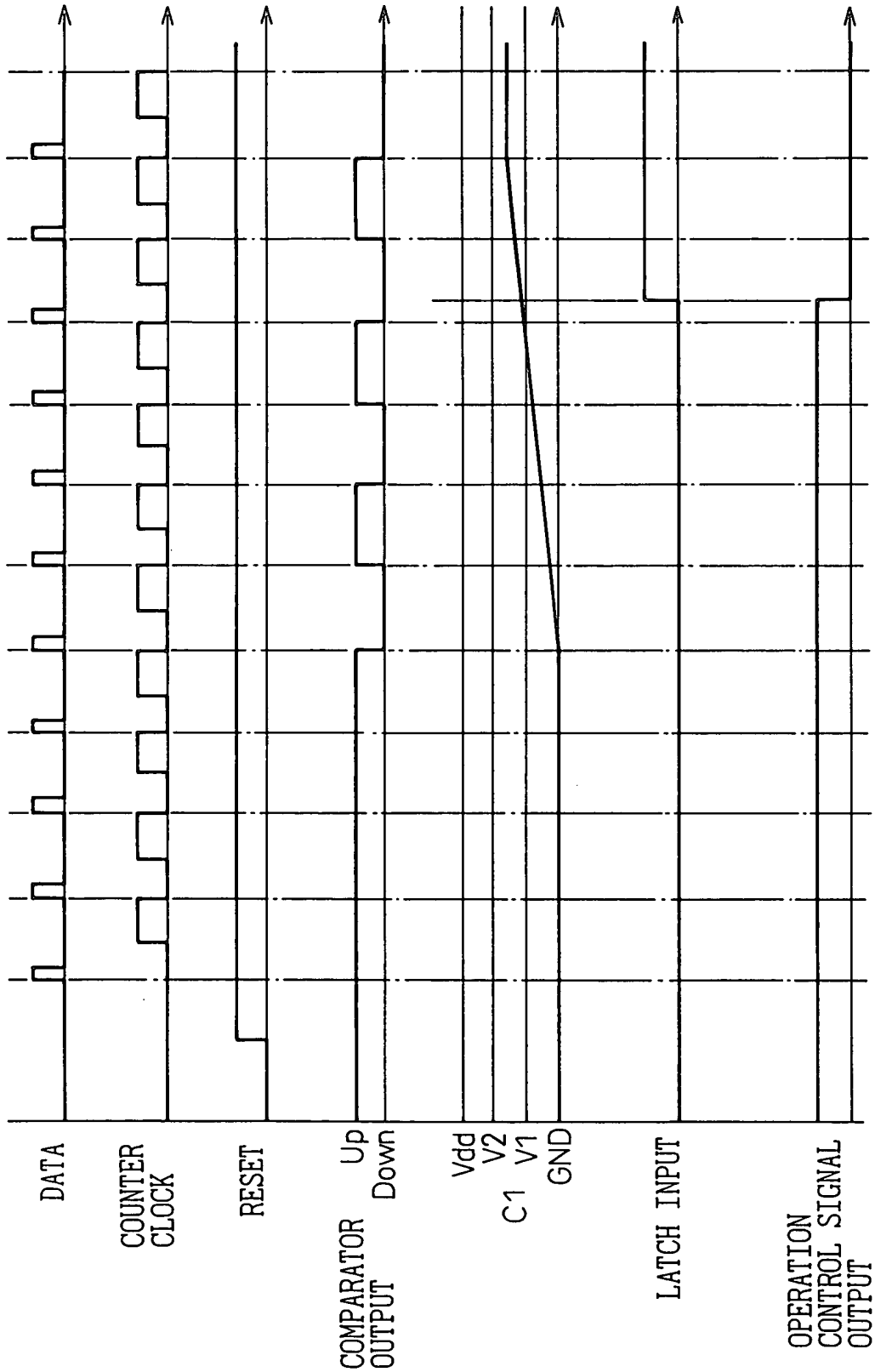

DATA
COUNTER CLOCK
RESET
COMPARATOR OUTPUT
Up
Down
Vdd
V2
C1
V1
GND
LATCH INPUT
OPERATION CONTROL SIGNAL OUTPUT

Fig.86

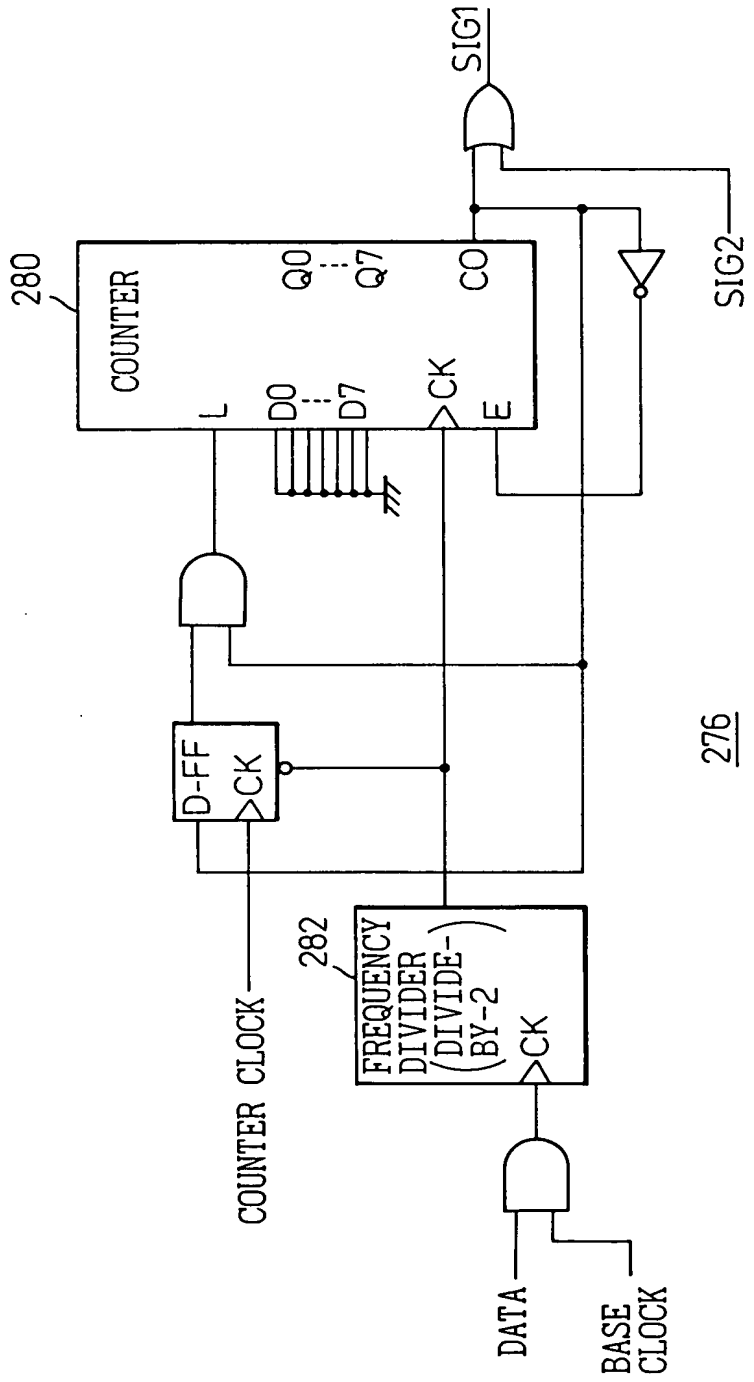

280
COUNTER
L
D0
D7
CK
E
Q0
Q7
CO
SIG1
SIG2
D-FF
CK
COUNTER CLOCK
282
FREQUENCY DIVIDER (DIVIDE-BY-2)
CK
DATA
BASE CLOCK
276

Fig.87

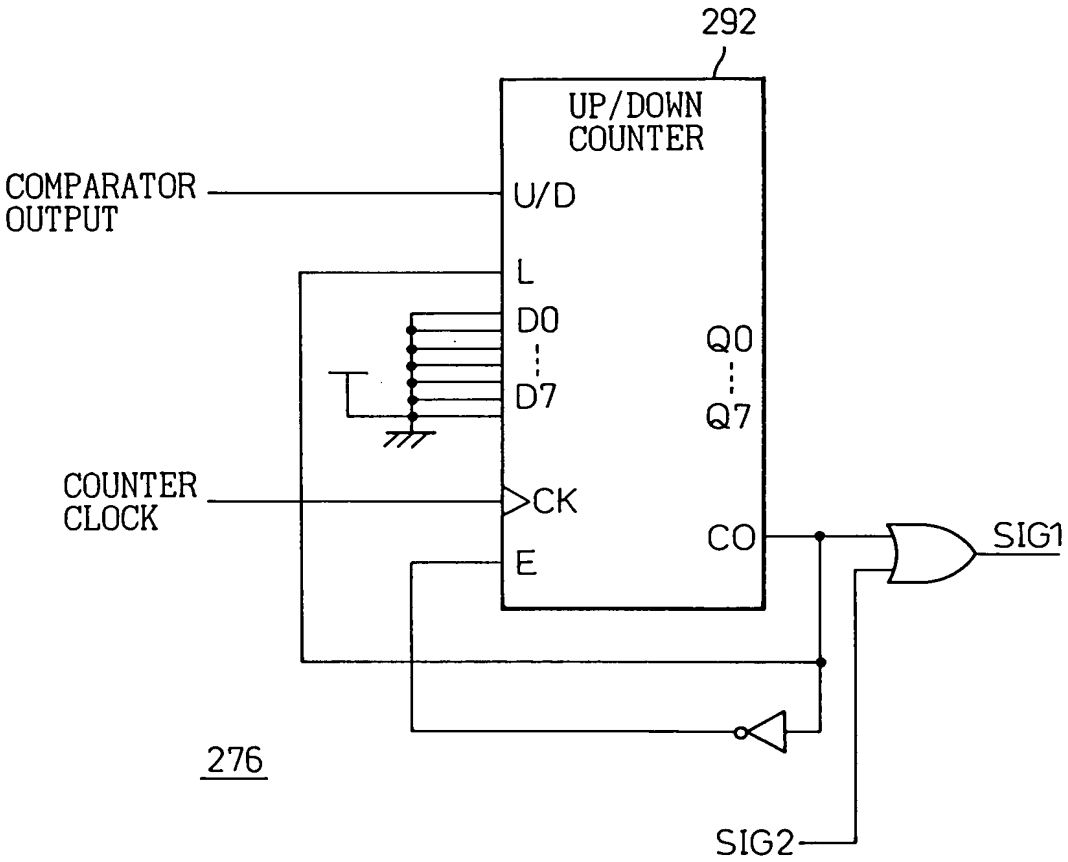

292
UP/DOWN
COUNTER
COMPARATOR
OUTPUT
U/D
L
D0
D7
Q0
Q7
COUNTER
CLOCK
CK
CO
E
SIG1
276
SIG2

Fig.88

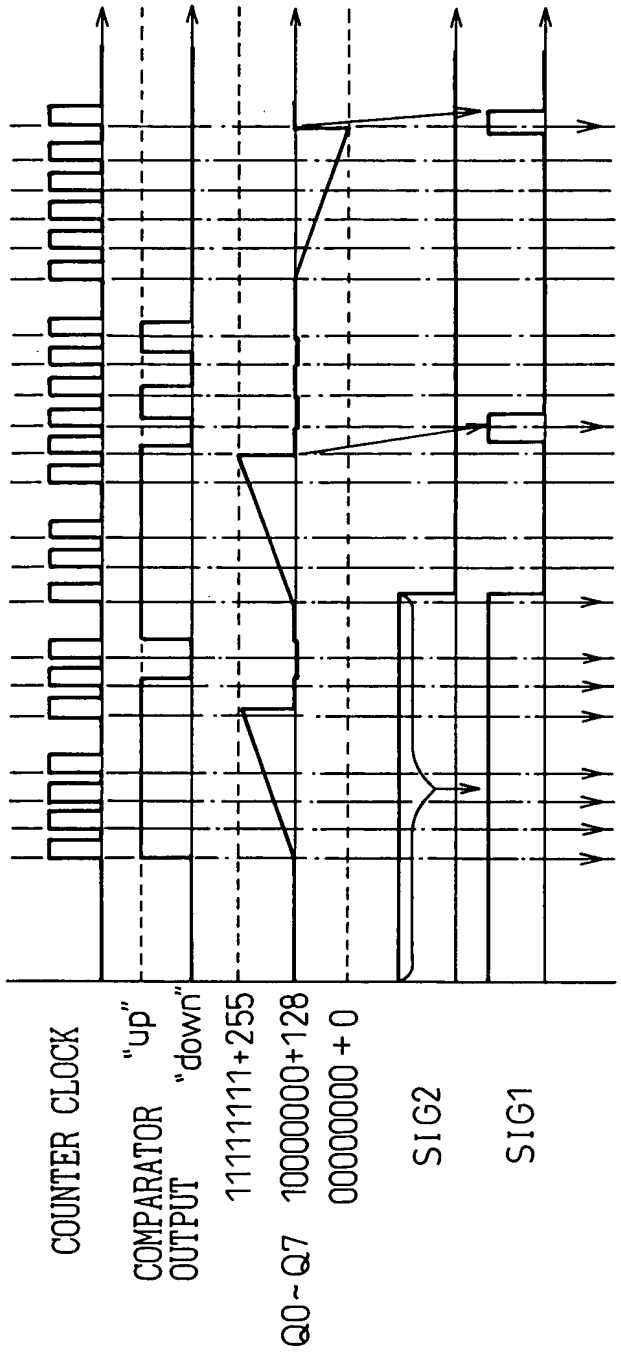

COUNTER CLOCK
COMPARATOR OUTPUT
"up"
"down"
Q0~Q7
11111111+255
10000000+128
00000000+0
SIG2
SIG1

Fig. 89

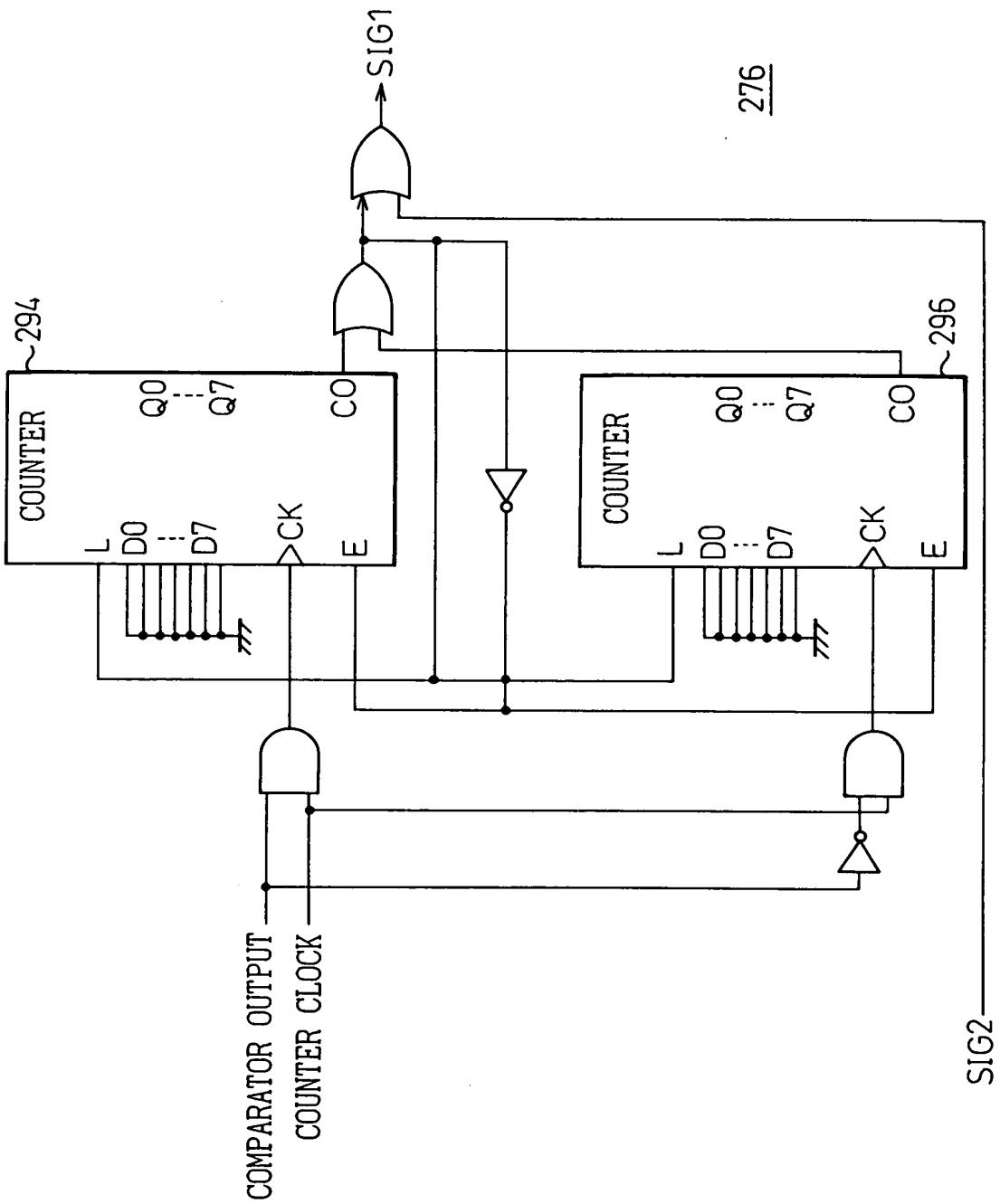

276
SIG1
SIG2
294
296
COUNTER
Q0
Q7
CO
L
D0
D7
CK
E
COMPARATOR OUTPUT
COUNTER CLOCK

Fig.90

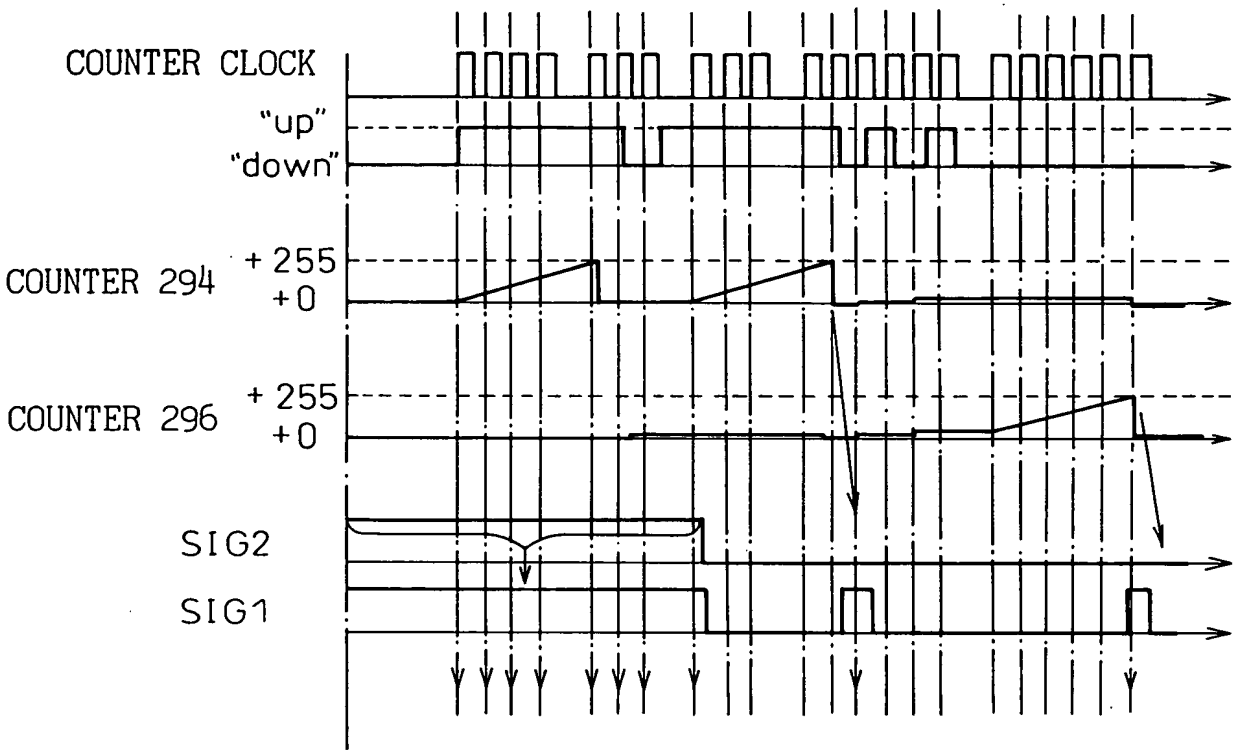
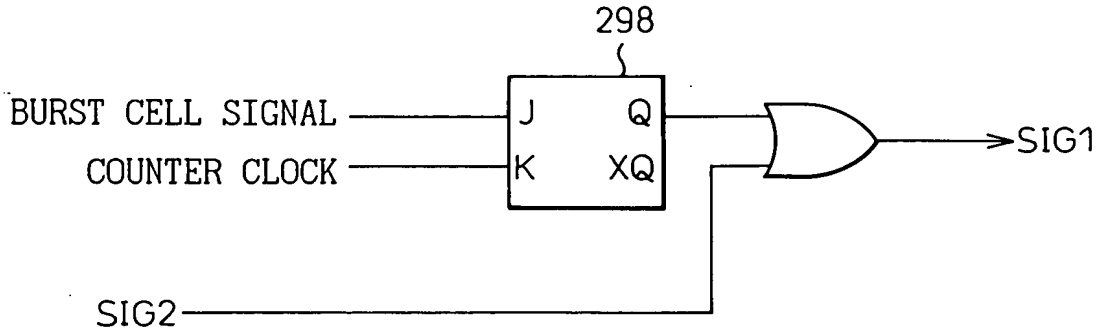
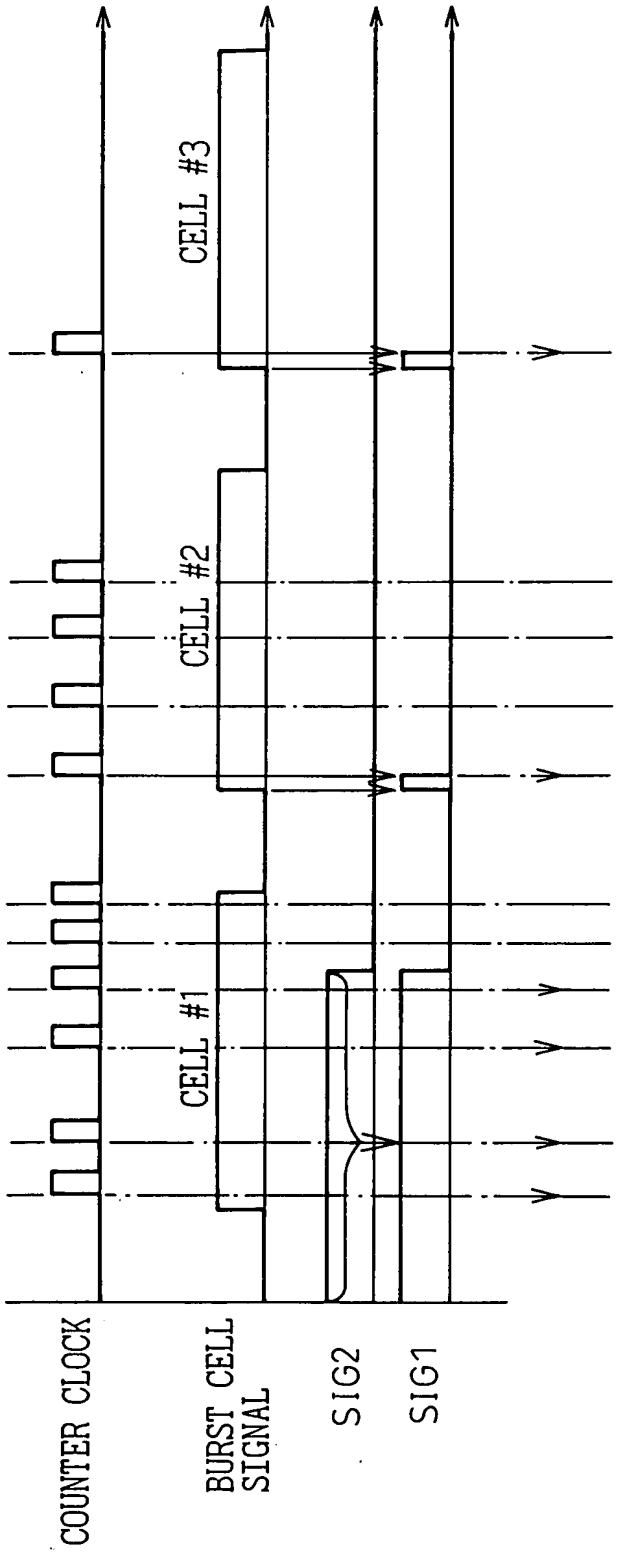



Fig.91




276

Fig.92


CELL #3
CELL #2
CELL #1
COUNTER CLOCK
BURST CELL SIGNAL
SIG2
SIG1